The Final Frontiers of Lithography Manufacturing

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October , 2009

國科會「伯樂計畫」 伯·樂·計·畫 Elite Project

PineBrook Imaging Systems (PBIMG)

Outline

- Lithography Manufacturing beyond 22nm
  - ArFi Double Patterning (DP)
  - SMO
  - EUV
- Alternative Lithography Manufacturing
  - Massively Parallel e-Beam
  - Nanoimprint
  - Through Silicon Vias (TSV)
- Moore’s Law & Lithography Manufacturing Roadmap

Lithography Beyond 22nm Node

- Leading Candidates
  - ArFi Double Patterning
    - Why sidewall spacer DP + gridded design rules?
  - EUV with OPC
    - Concerns with source, system, mask, & resist
- Additional Candidates
  - Massively Parallel e-Beam Direct Write
    - Throughput, throughput, throughput
  - Nanoimprint
    - 1X mask quartz defect is hard to repair

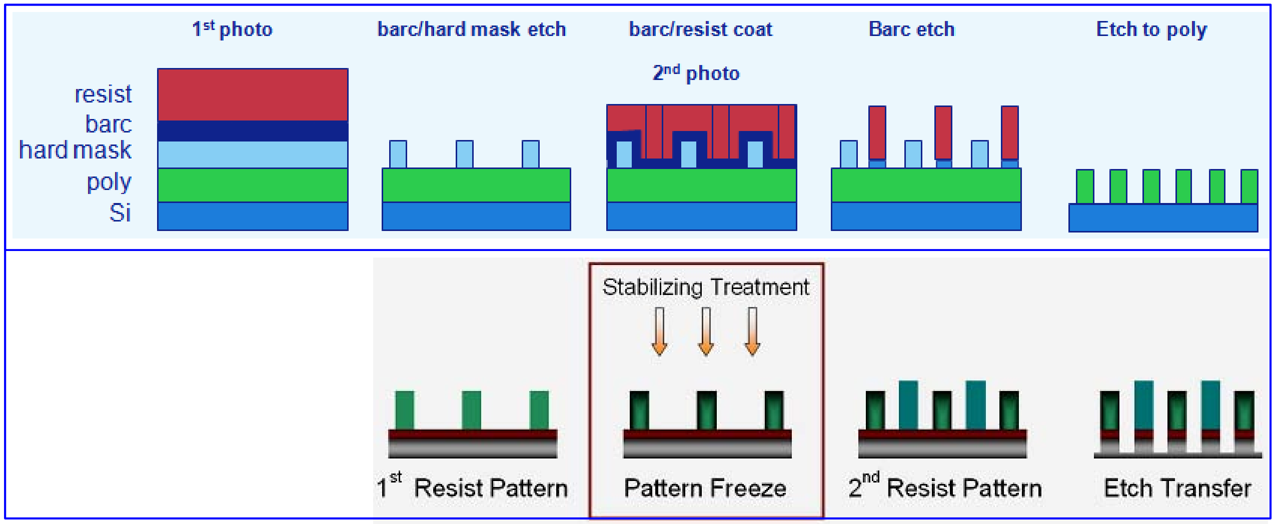
Which Double Patterning Method?

- Three DP methods are being investigated –
  - Litho-etch-litho-etch (LELE)
  - Litho-freeze-litho-etch (LFLE)
  - Sidewall Spacer Double Patterning, or Self Aligned Double Patterning (SADP)

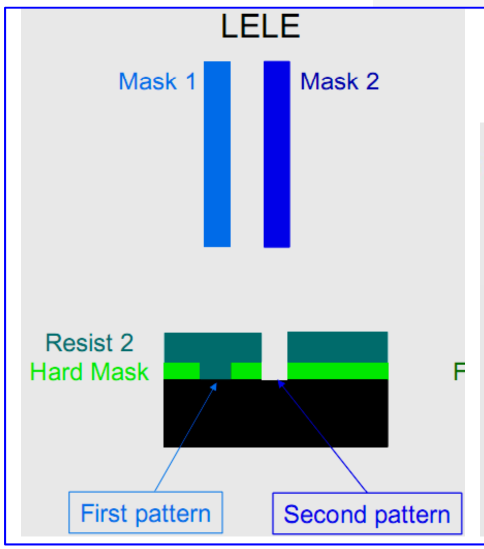
LELE vs. LFLE (Different Trench Coloring)

LELE – Clear field for lines

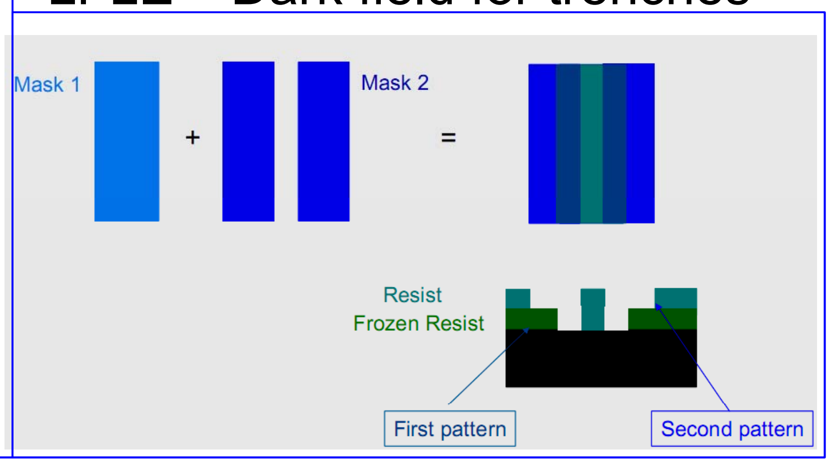
LFLE – Clear field for lines



LELE – Dark field for trenches



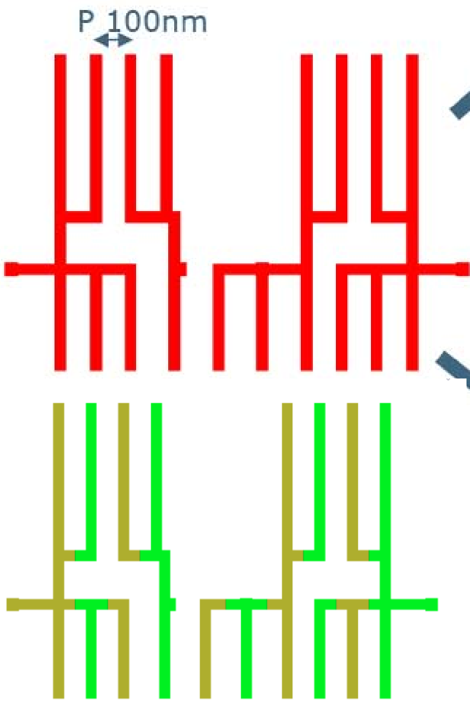
LFLE – Dark field for trenches



JC Park, et al, MaskTools, Oct, 2006
T. Wallow, Global Foundry, July 2009

Double Patterning Demonstration

TARGET
Min Pitch 100nm
k1 = 0.31

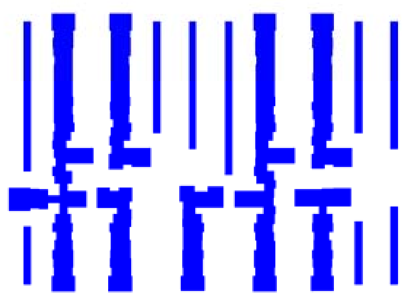


JC Park et al, MaskTools, 2006 BACUS

SPLIT + OPC

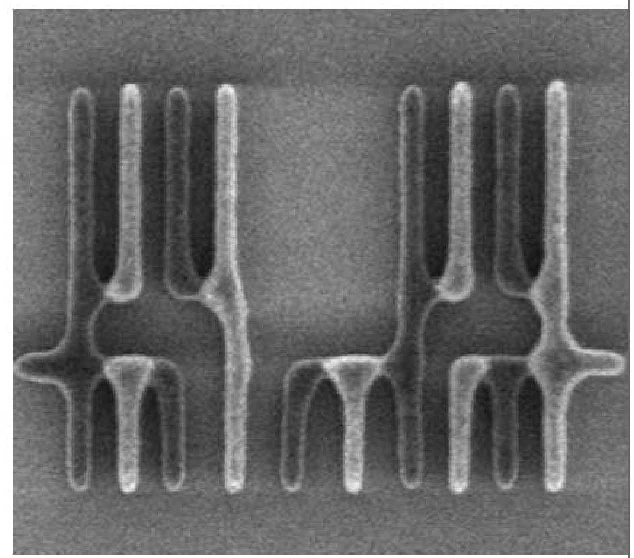
MASK A

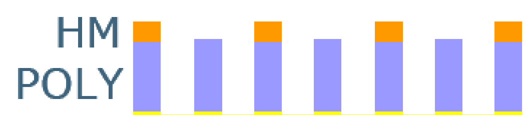
MASK B



G. Vandenberghe, IMEC, Feb, 2008

POLY PATTERNING
Annular 0.8/0.5
X-Y polarized
193i - 1.2NA





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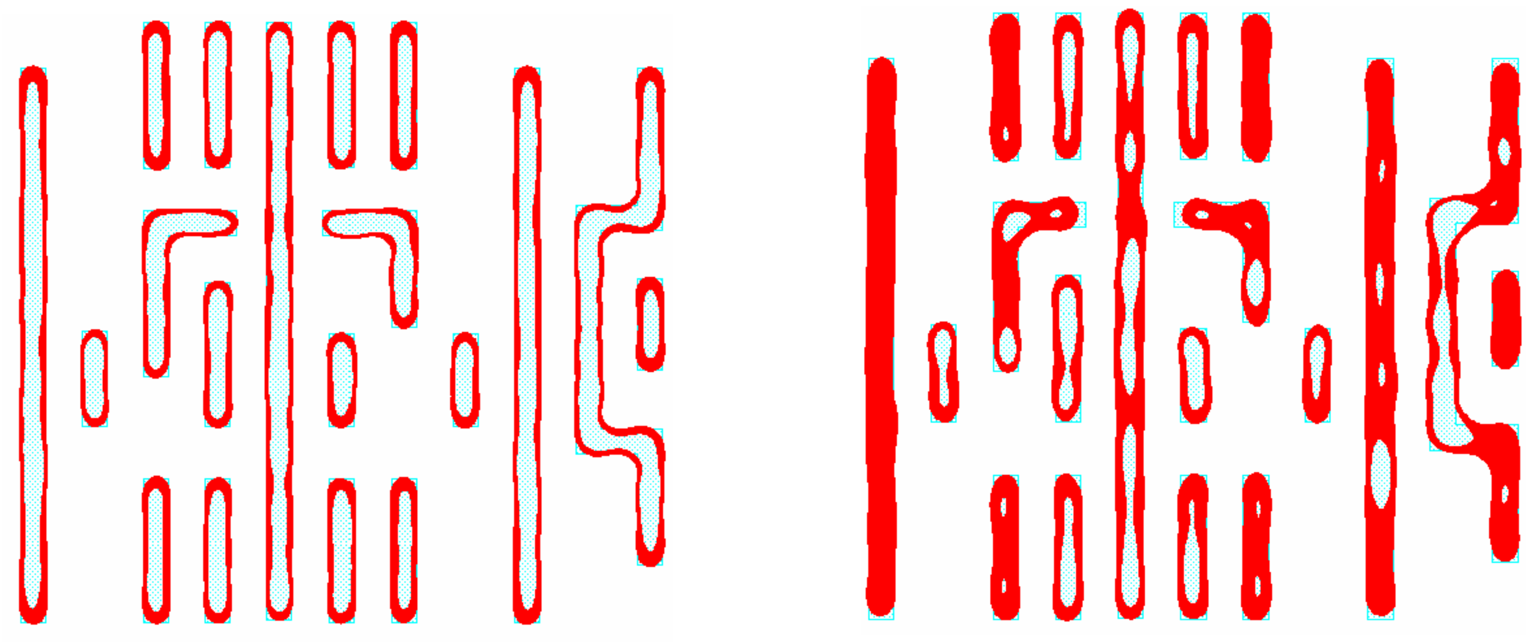
PineBrook Imaging Systems Corporation

Very low k1 lithography has low aerial image contrast

→ lots of unacceptable “2D hot spots”

→ little margin of error tolerance even with well-calibrated model OPC

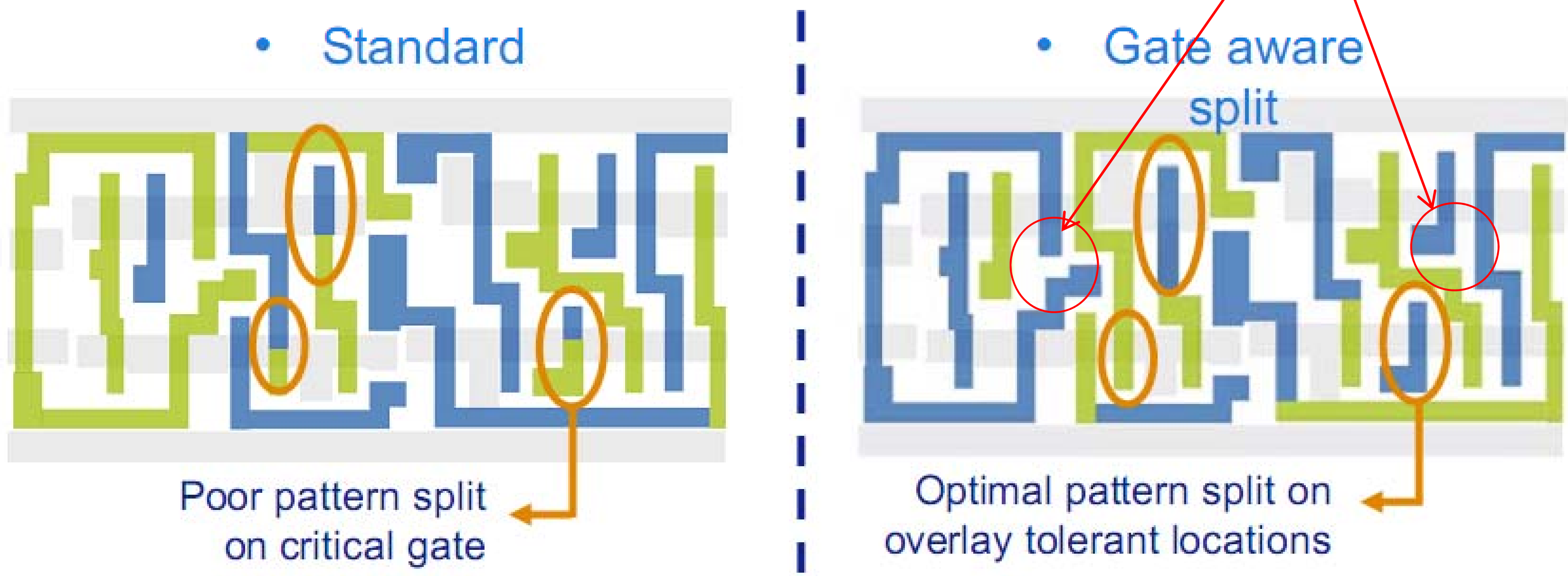


$k_1 = 0.35$ $k_1 \sim 0.3$

Source: T. Wallow, Global Foundry, July 2009

No optimized solution in Double Patterning for 2D features

→ may be good for overlay but not "2D hot spots" in areas with low aerial image contrast



DP example from S. Miller, ASML, July 2009

To enable double pattering lithography for High Volume manufacturing

- Restrict 2D features to exist within the optical proximity range with their 1D neighbors
- Not to create additional 2D features
- Convert the all IC designs to 1D regular pitch layout
  - Yes, design rules must be restrictive and on-grid
- Use “cut mask” to produce 2D features
  - Yes, we will need one more exposure

Sidewall Spacer Double Patterning

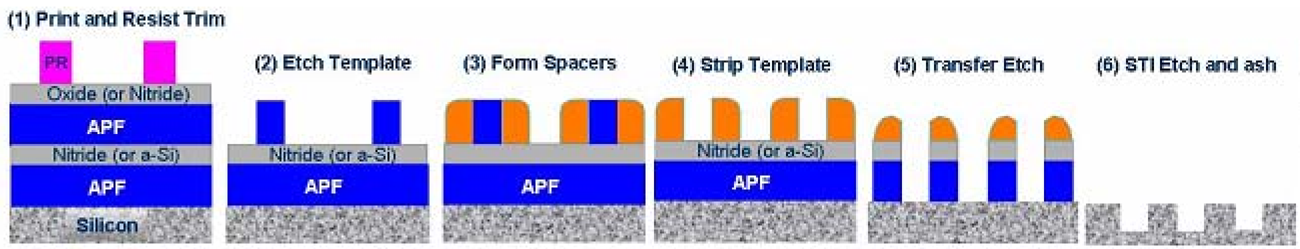
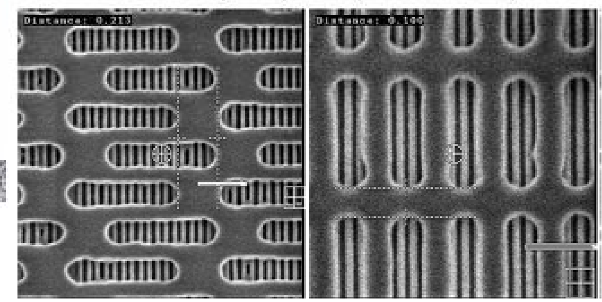


Figure 2: Illustration of process flow for generating 22nm STI array.

Via links superimposed (without BARC)



Cut masks patterned over the 22nm STI array.

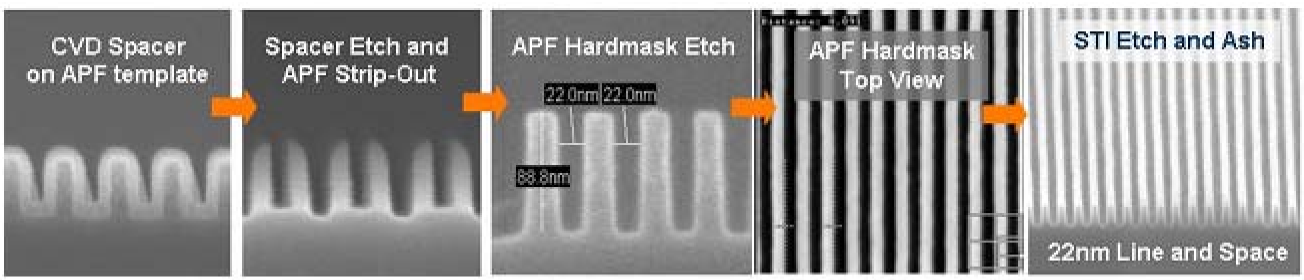
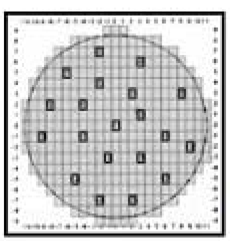
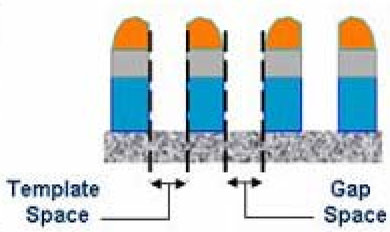


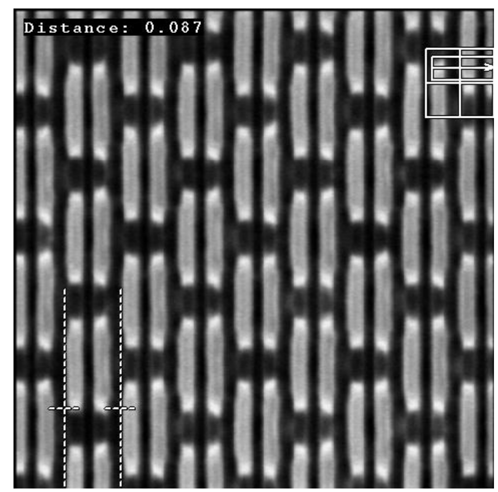
Figure 3: SEM image snapshots throughout process flow.





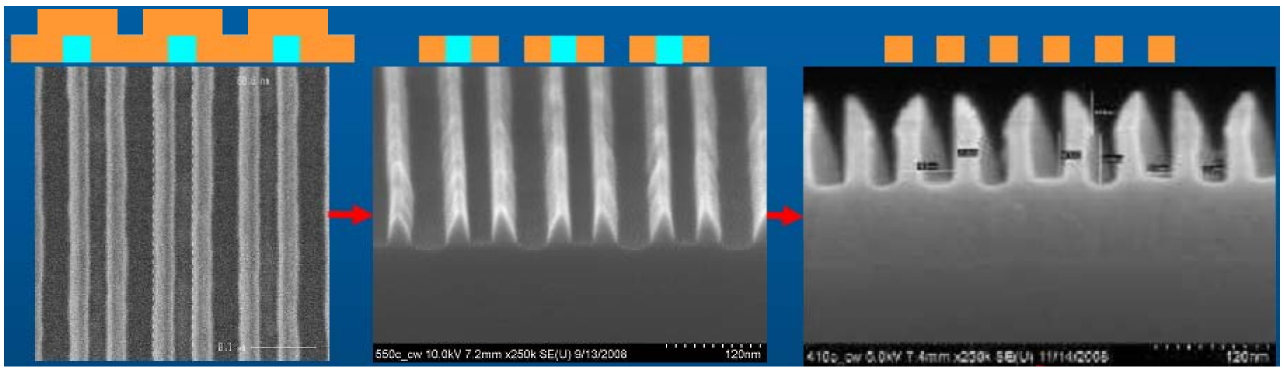
	Template Space	Line	Gap Space	LER	LWR
Mean (nm)	24.7	22.5	22.7	1.5 nm	1.6 nm
3 Sigma (nm)	2.0	1.1	2.5		

M. Smayling et al., Tela Innovations, Inc., SPIE 2008

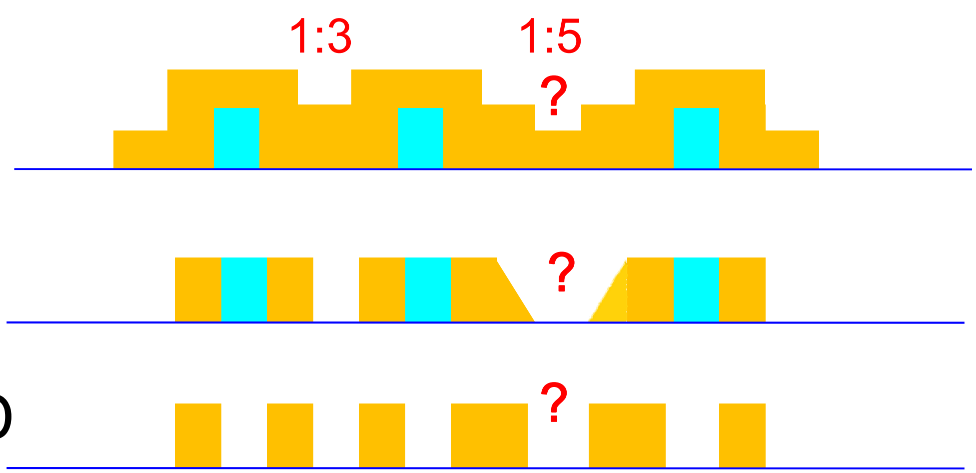


SEM of 11nm node SRAM structure (22nm half-pitch) demonstrates scalability of SADP technology.
(Source: Applied Materials, 2008)

1:3 Line:Space Design Rule Required for Sidewall Spacer DP



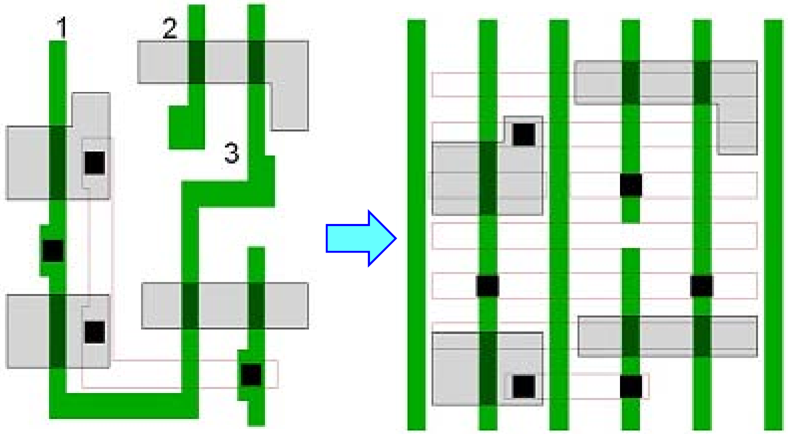
“Forbidden” gap could be created due to thin film deposition at different space area, subsequently causing uncontrollable CD



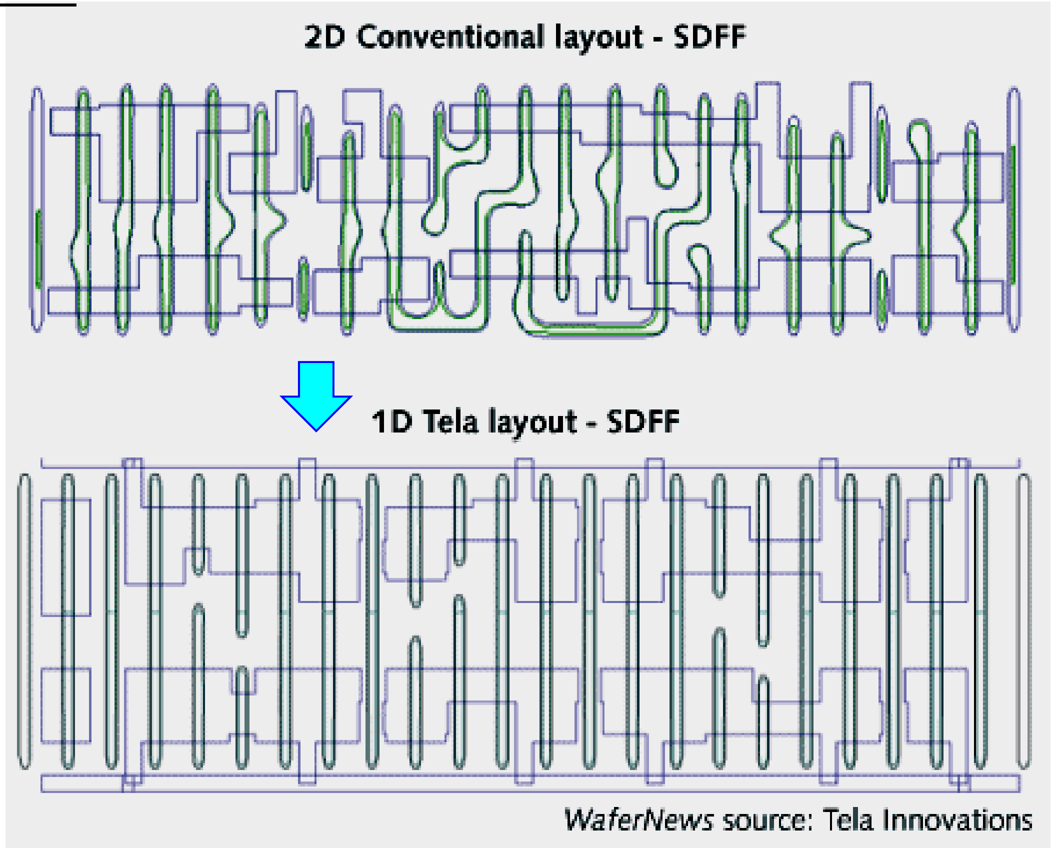
Converting conventional 2D IC design to 1D regular pitch with unidirectional feature layout

Design rules for sidewall spacer DP

1) 1D regular pitch layout
2) Unidirectional feature
3) Line: space = 1:3



R. T. Greenway, PAL, 2009 SPIE

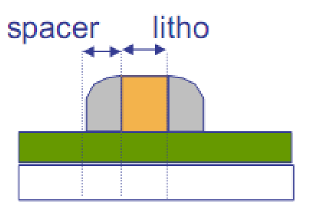


M. D. Levenson, Microlithography World, February, 2008

Double Patterning Manufacturing Considerations
Sidewall Spacer vs. LELE and LFLE

Sidewall Spacer DP has less demanding overlay requirement

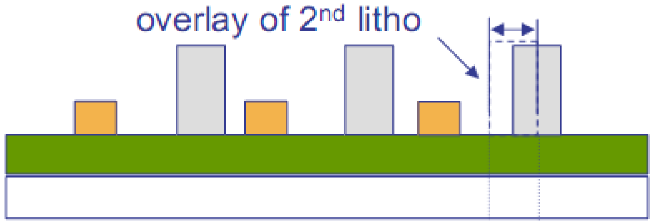
Spacer deposition in total CDU
→ CDU(litho) main enabler



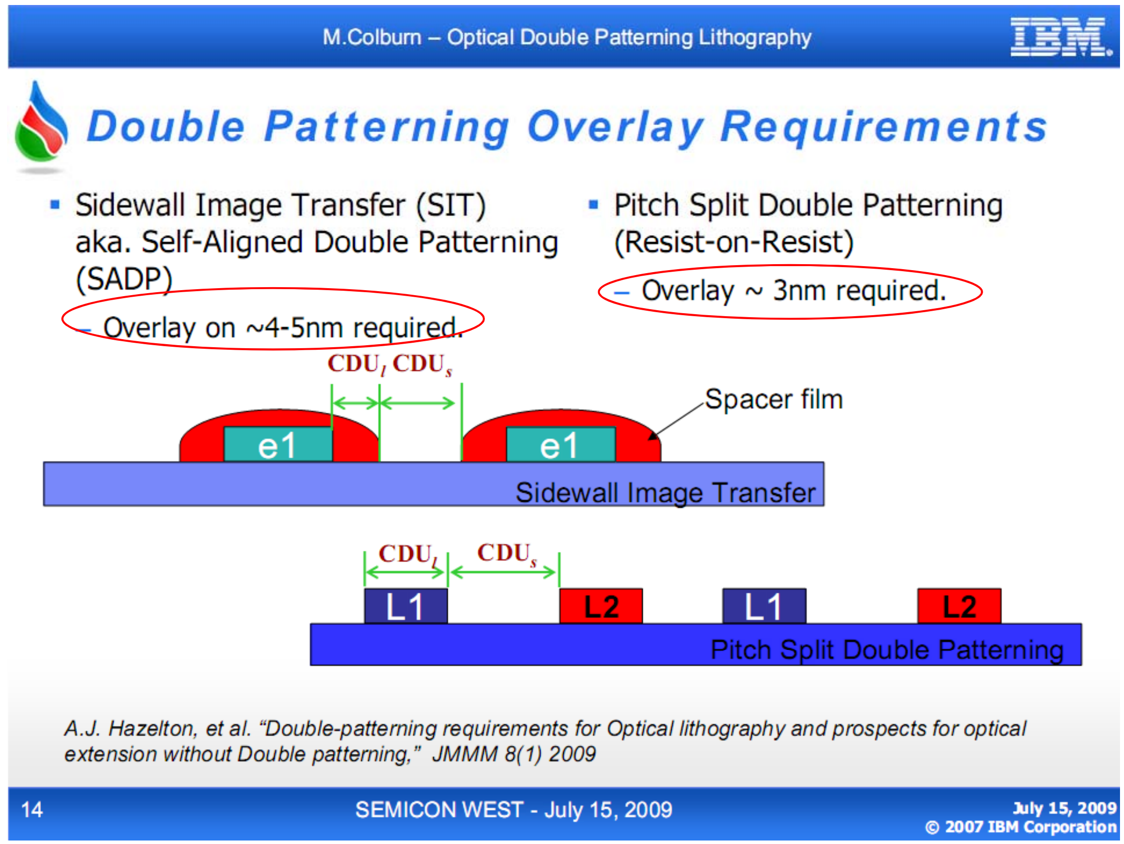
CDU depends on litho and
on spacer deposition

Overlay and CD uniformity are entangled
→ Overlay becomes enabler for CDU

Space width depends on
overlay of 2nd litho

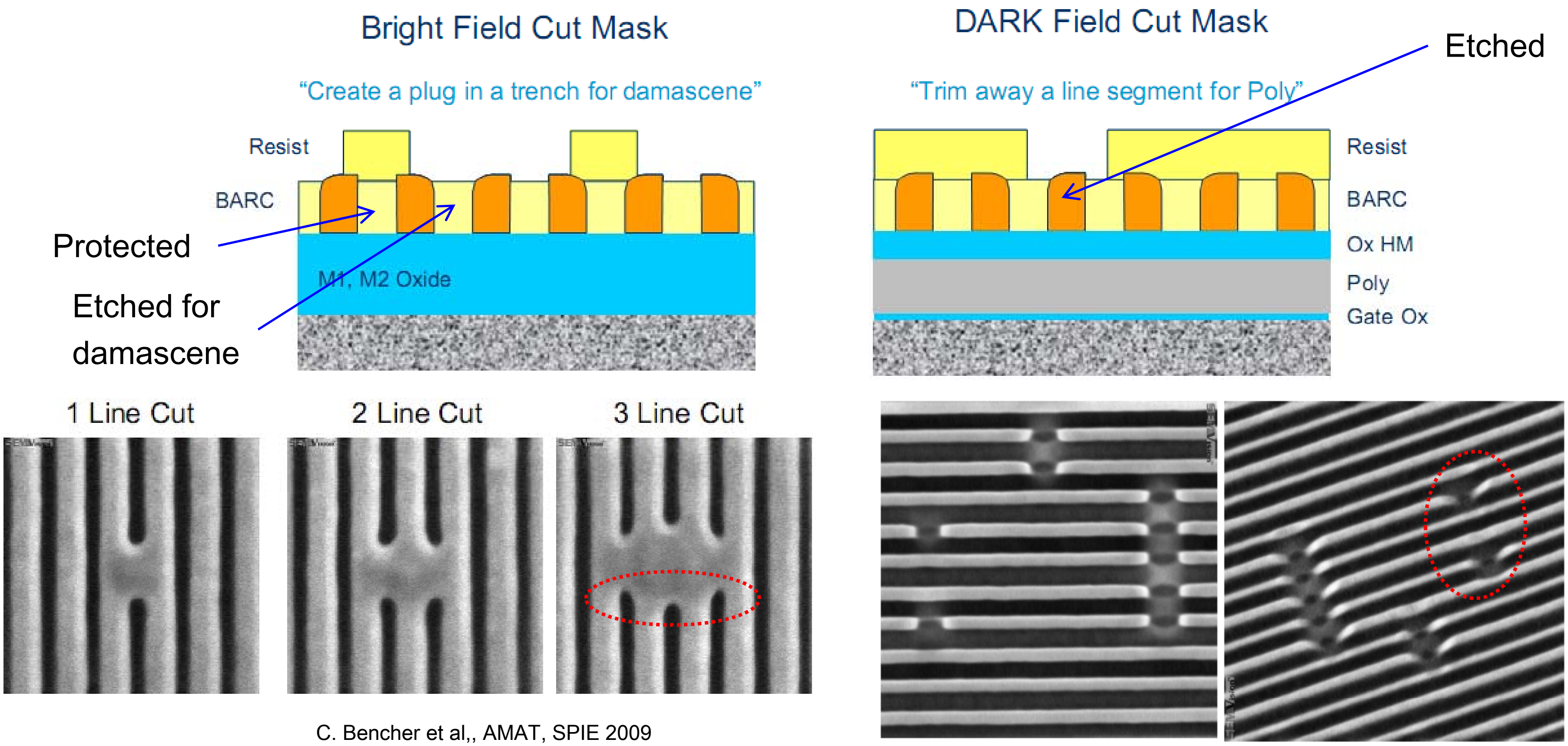


B. Arnold, ASML, July, 2008



Sidewall Spacer Double Patterning –

1) Feasible for both Gate & Damascene Metal Trench Masks
2) Must apply OPC to correct end-tapering of the "cut-mask" patterns
3) Sophiscated "Cut Mask" patterns are expected to be used for actual manufacturing



C. Bencher et al,, AMAT, SPIE 2009

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DP for High Volume Manufacturing (HVM)

Sidewall Spacer is the best method for DP HVM → must enforce design rules for 1D regular pitch w/ unidirectional feature layout

Double Patterning Method	Sidewall Spacer	LELE	LFLE
CDU control factors?	Imaging	Imaging and Overlay	Imaging and Overlay
Cut Mask?	Yes	Not necessary	Not necessary
Require 1D regular pitch w/ unidirectional feature layout?	Line: space = 1:3 to get 1:1 DP	Not necessary but can be beneficial	Not necessary but can be beneficial
Coloring (pitch splitting) algorithm	Can be rule based with model OPC	Model-based pitch splitting with aggressive model OPC	Model-based pitch splitting with aggressive model OPC
Applicable to both line and trench patterns?	Yes	Yes	Yes, but more complicated pattern decomposition for trench than LELE
Imaging Scalability (tech node?)	k_1<0.15 (15nm node possible?)	k_1<0.20 (sub-22nm possible?)	k_1<0.20 (sub-22nm possible?)

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  - SMO and Contact Hole Imaging
  - EUV
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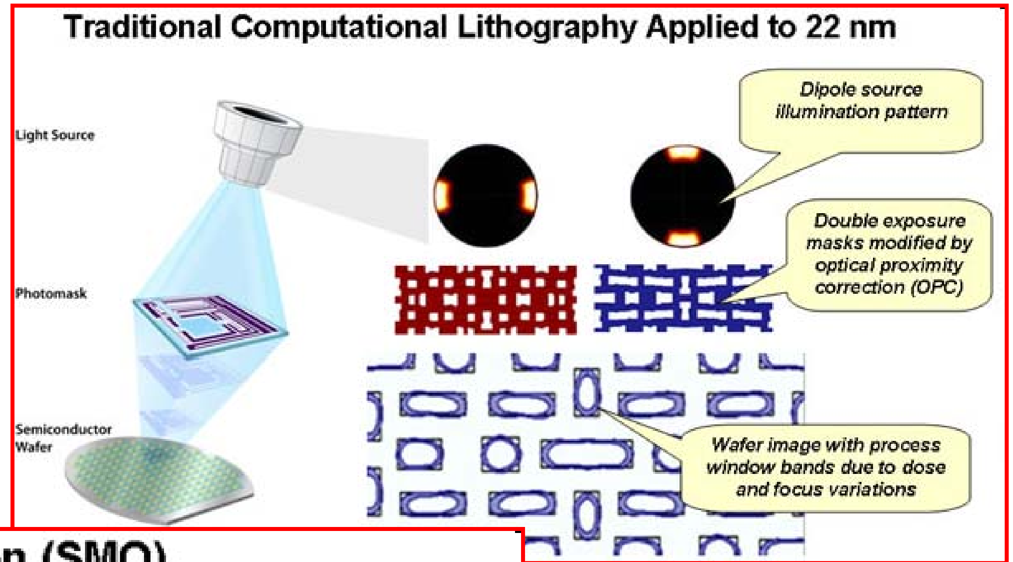
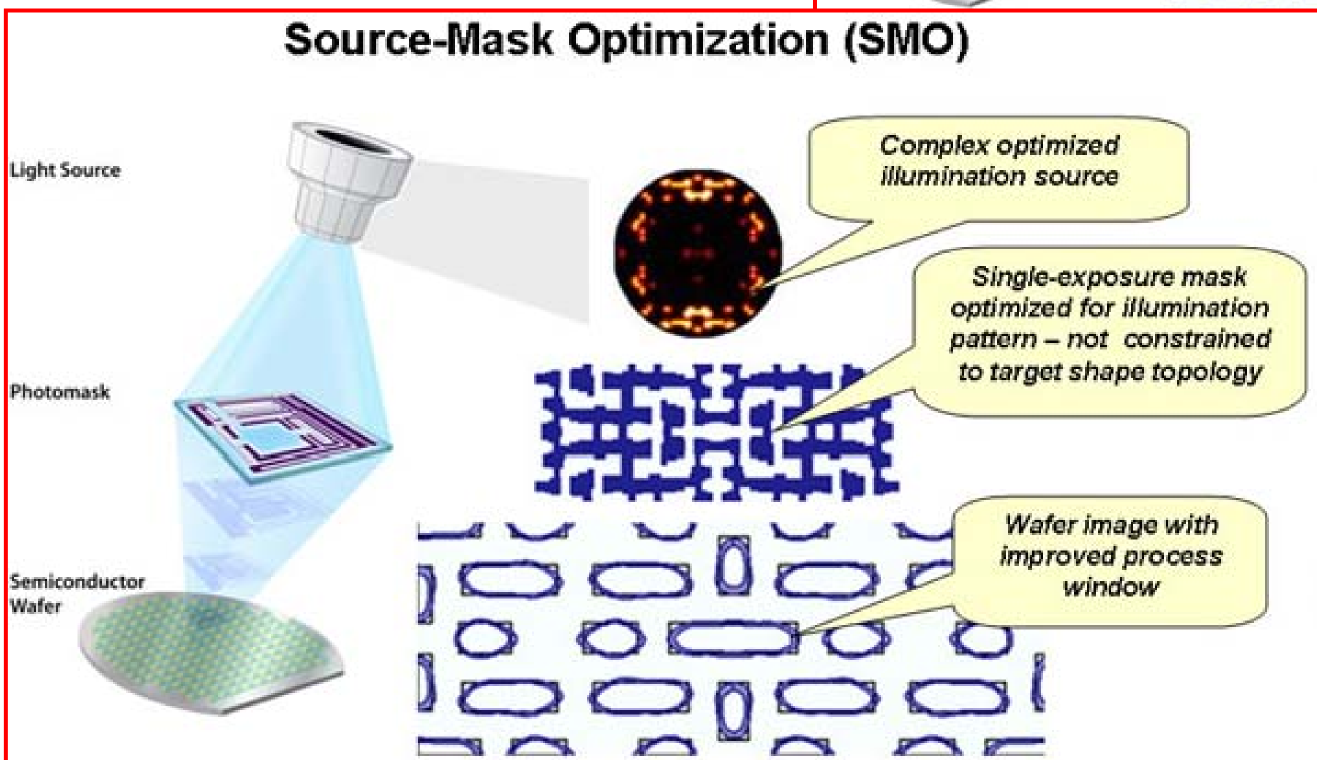
SMO – complex illumination source + unique OPC mask design unconstrained





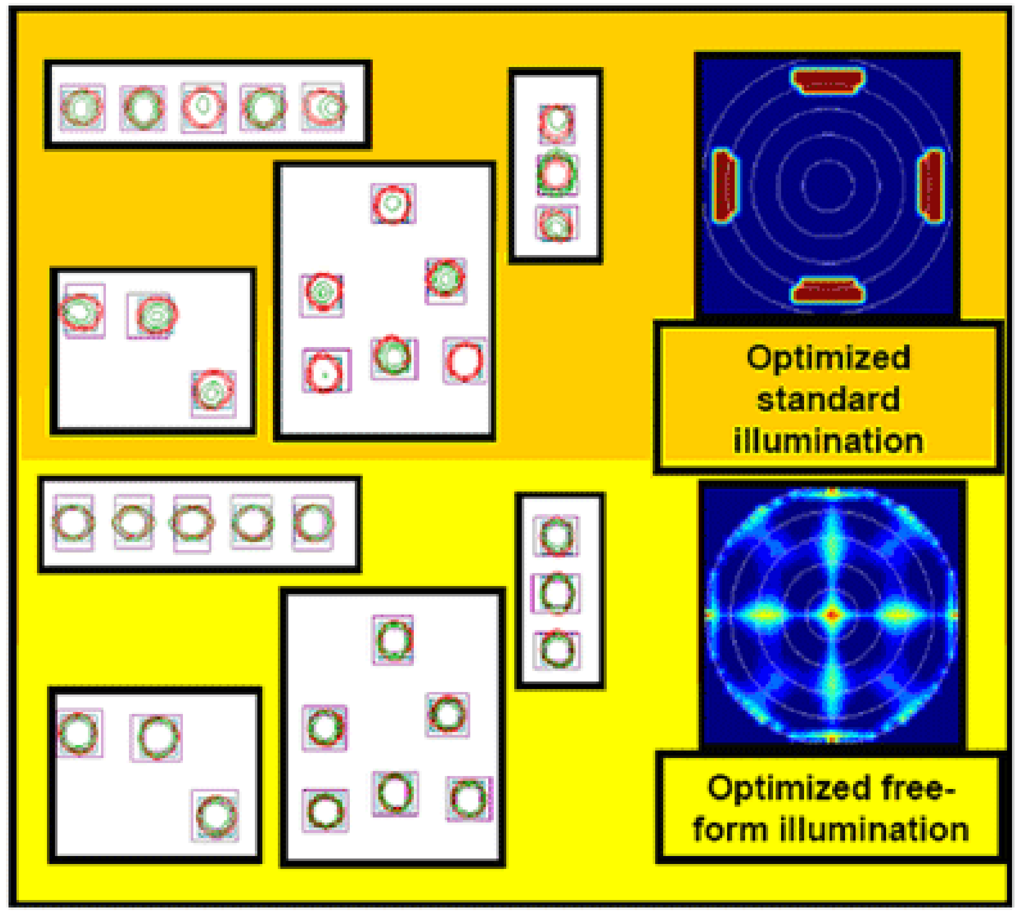
Facts about SMO:

1) Improve more on exposure latitude but not DOF, very small process margin.
2) Must be enabled by restricted design rule.

(Source: IBM, published by Semiconductor International, 9/18/2008)

Optimum SMO Requires Gray Tone Complex Illumination Source

- Source-mask optimization is an iterative approach
  - Get optimum custom illumination source + mask design
  - Improve in process window (more on exposure latitude)
  - Restricted design rules



[redacted]

(Source: Cadence, published by Semiconductor International), 2008

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EUV Outline –

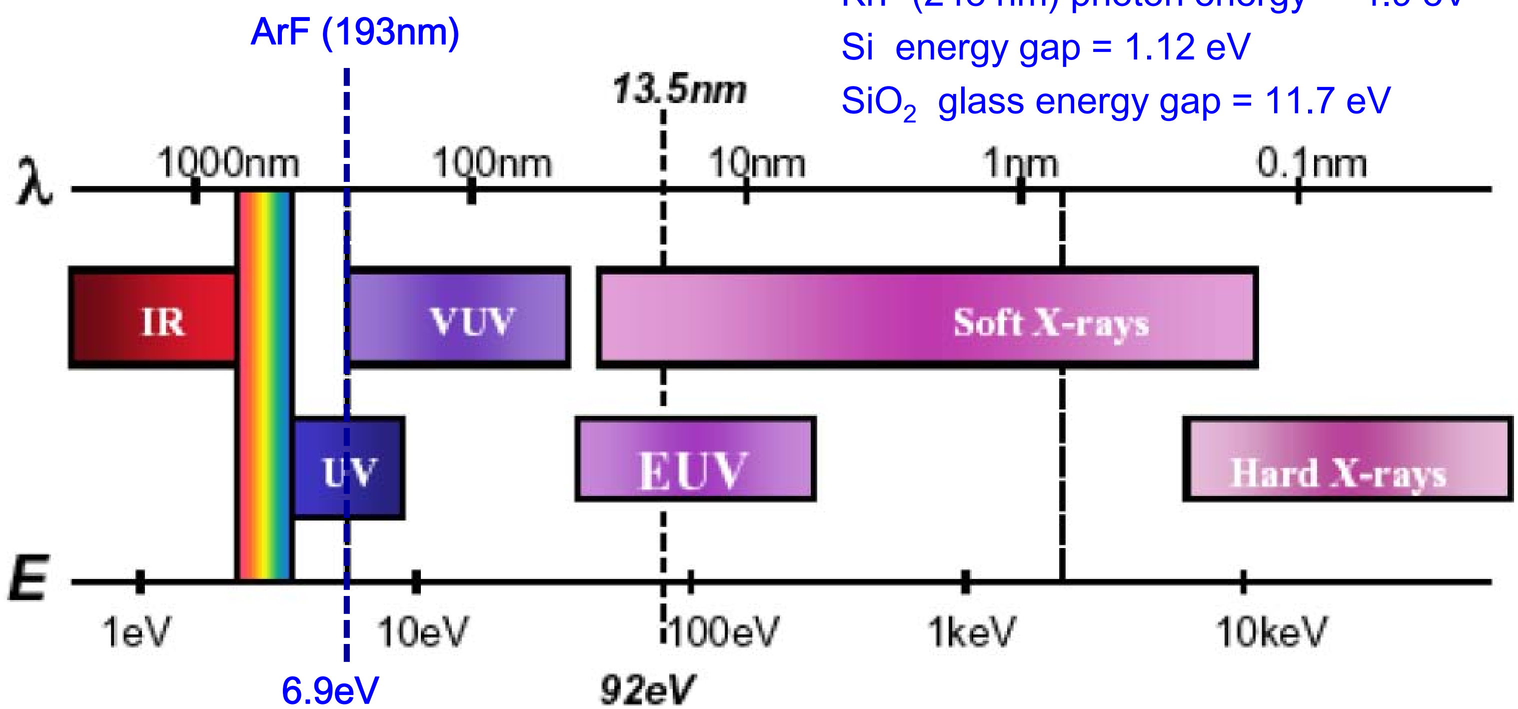
- What is EUV? EUV Source?
- EUV Scanner Optics
- EUV Mask
- EUV Resist
- COO for EUV vs. ArF DP
- EUV is coming but when?

What is Extreme UV (EUV)?

- EUV is a form of Soft X-Rays
- EUV photon is absorbed by all material & gases
- EUV imaging is reflective (mirrors) & under vacuum
- EUV reticle is also reflective, no pellicle is feasible

EUV photons are X-ray photons， absorbed by absolutely everything.
→ EUV exposure must be done in vacuum!

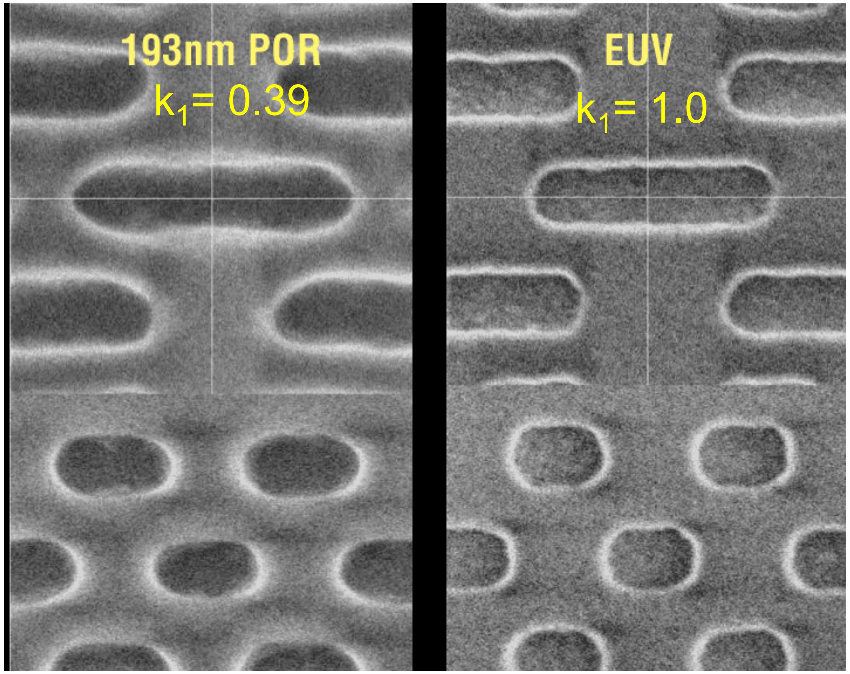
KrF (248 nm) photon energy = 4.9 eV
Si energy gap = 1.12 eV
SiO_2 glass energy gap = 11.7 eV



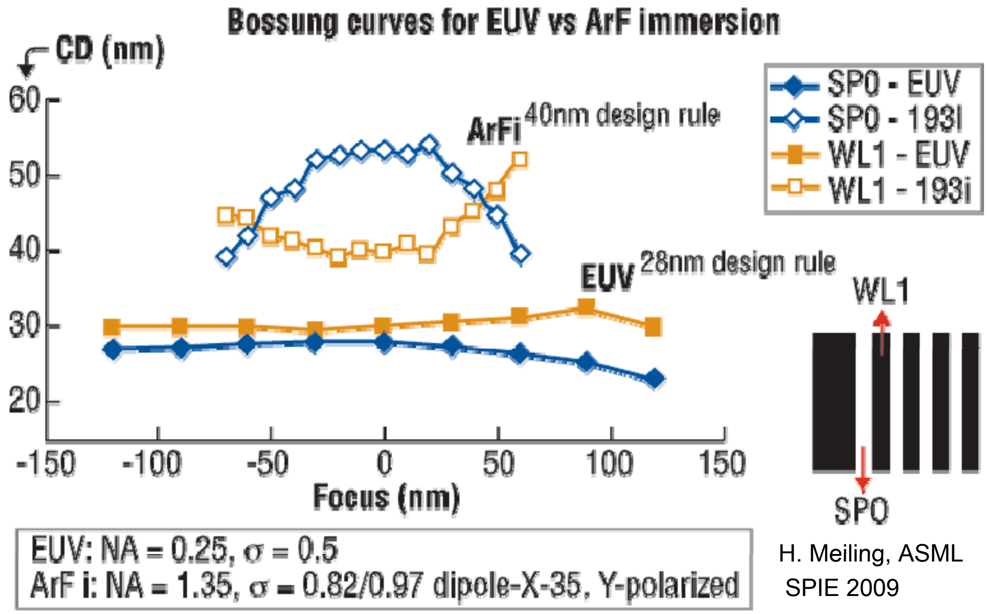
Extended from G. Vandenberghe, IMEC, Feb, 2008

Image Quality Comparison ArFi vs. EUV

Example here from Intel recently is not entirely justifiable, however.



G. Vandentop, Intel, SPIE 2009



H. Meiling, ASML
SPIE 2009

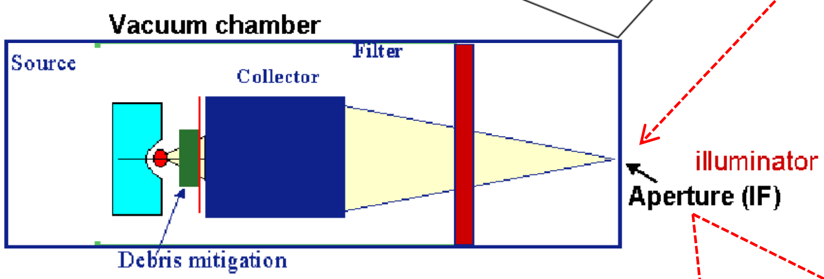
EUV has less corner rounding for staggered trenches, but at 112.5nm pitch for Intel's 32nm node, it does not justify EUV

EUV has a much larger process window at lower k_1, more suitable for making NANA flash device beyond 28nm node

EUV Source

Requirement EUV power (W)
115 W @ 5 mJ/cm2
Or, 180 W @ 10 mJ/cm2
Repetition frequency (kHz) >7-10 kHz

Source specifications are defined at intermediate focus (IF), which is the illuminator entrance



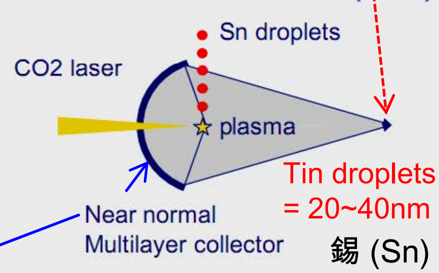
V. Bakshi, EUV Litho, July 2009

LPP is preferred since it can better collect energy and direct it to the intermediate focus (IF) position.

Cymer reported in press release July 13, 2009, 75 W power with possibility of 100W in Q3 2009.

Courtesy of Cymer

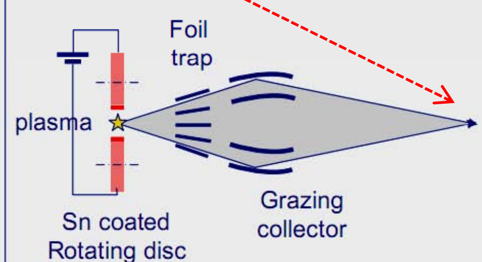
Laser-Produced Plasma (LPP)



CO_2 laser ignites Sn plasma
Debris mitigation by gas, …

Near normal incidence collector

Electrical Discharge (DPP)



High voltage ignites Sn plasma
Debris mitigation by foil trap

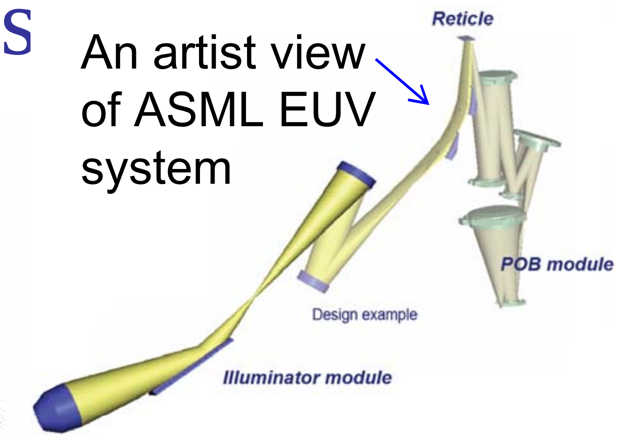
Grazing incidence collector

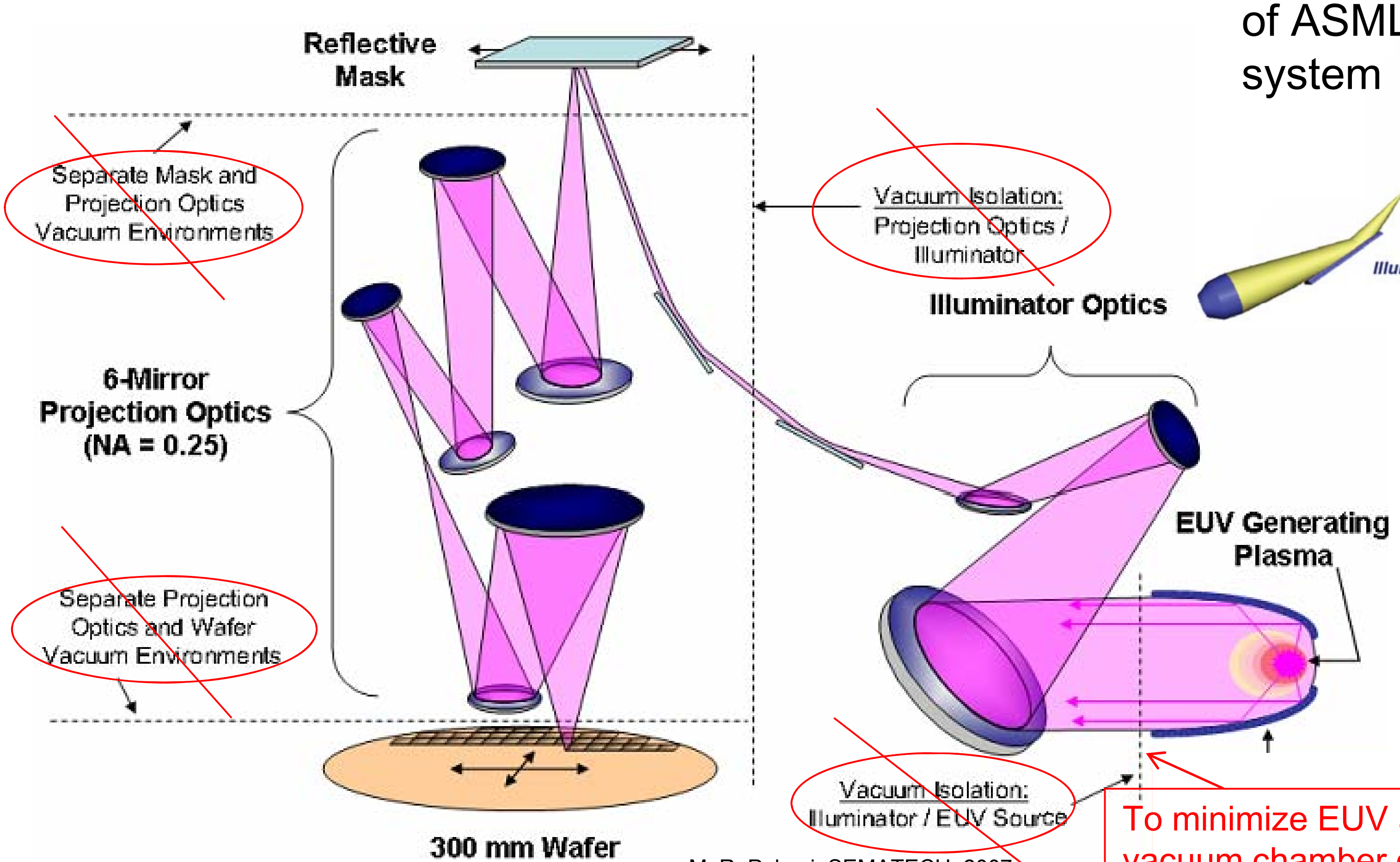
Hans Meiling, ASML, July 2009

Future of DPP is uncertain as Tin LPP has been chosen by ASML for beta tools.

A Conceptual View for a 0.25NA EUV Scanner with 6 Mirror Elements

An artist view of ASML EUV system





M. R. Polcari, SEMATECH, 2007

To minimize EUV absorption, none of vacuum chamber can be separated. EUV exposure must be done in one big vacuum chamber!

No Pellicle Possible for Reflective EUV Mask

- EUV mask handling could be done in sealed vacuum carrier
  - Less concern for reticle handling
- But not possible to avoid debris produced by source and ions during exposure, because
  - Source chamber cannot be physically separated from imaging optics chamber

EUV Contaminations on Lens and Mask –

→ Degrade lens mirror reflectivity and life time

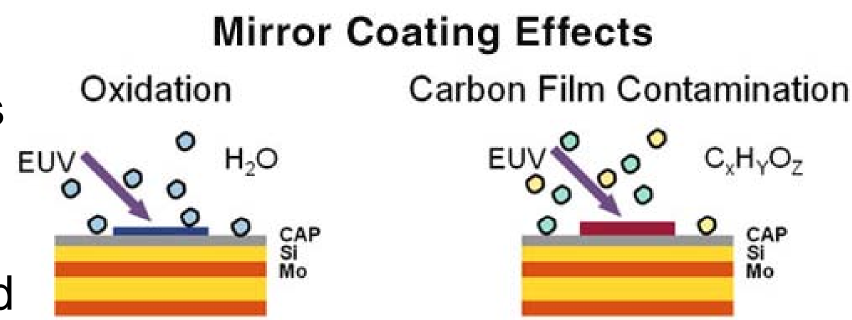
→ Dose required to CD target can be changed!

2 EUV lens mirror contamination mechanisms –

1) Oxidation degradation is irreversible

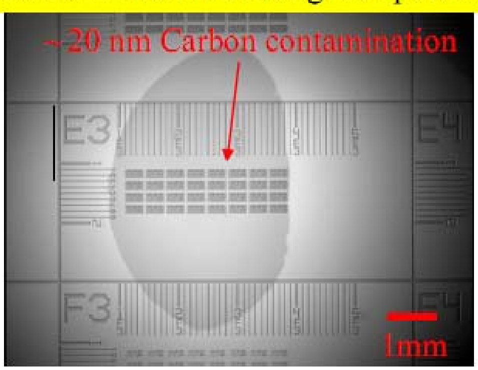
   Need to use anti-oxidation capping layers
   → when building the mirror

2) Hydrocarbon film deposition due EUV resist outgassing. → This can be cleaned by using oxygen gas under EUV radiation

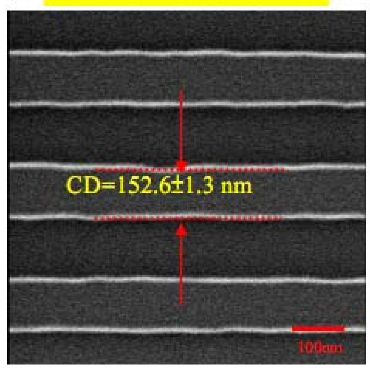


T. Miura et al., Nikon Precision Inc., Semiconductor International, Nov, 2008

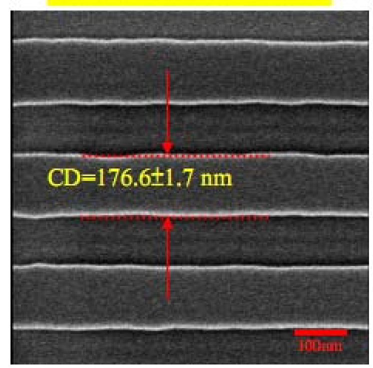
Contaminated with designed aperture



Before contamination



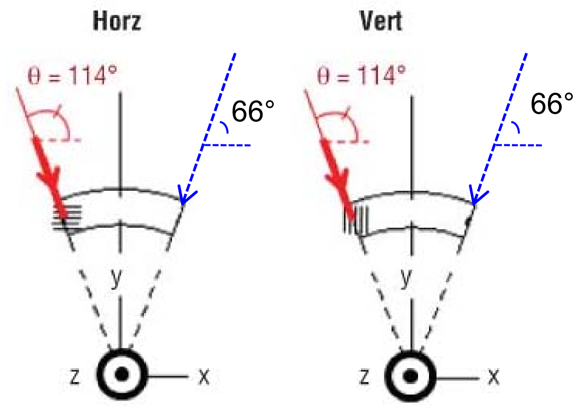
After contamination

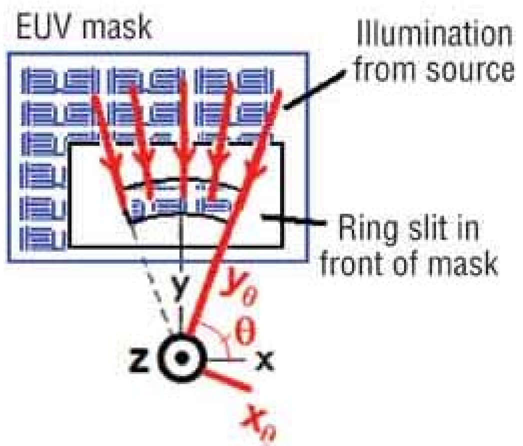


Observed larger mask CD after contamination!

G. Denbeaux, University at Albany, July 2009

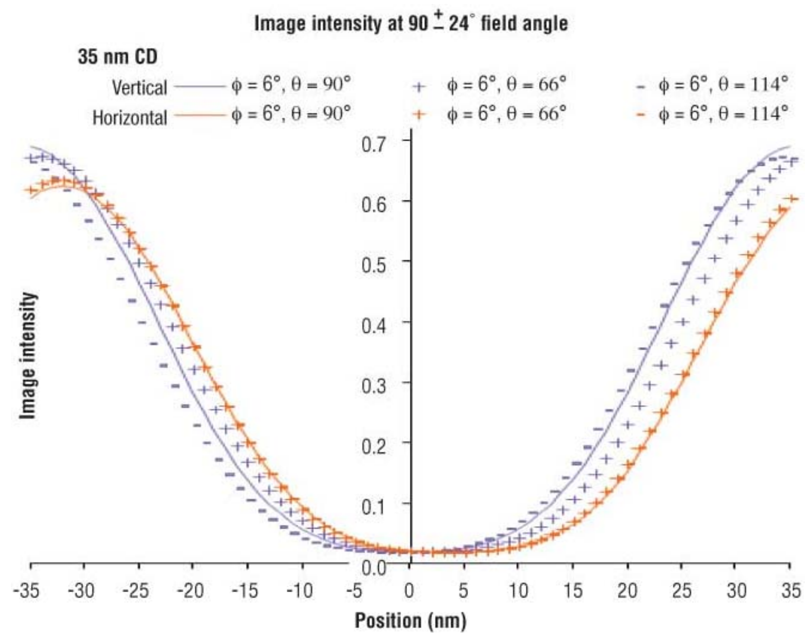
EUV Scanning Ring Field Must Correct for H-V CD Variation





90° – center of ring field

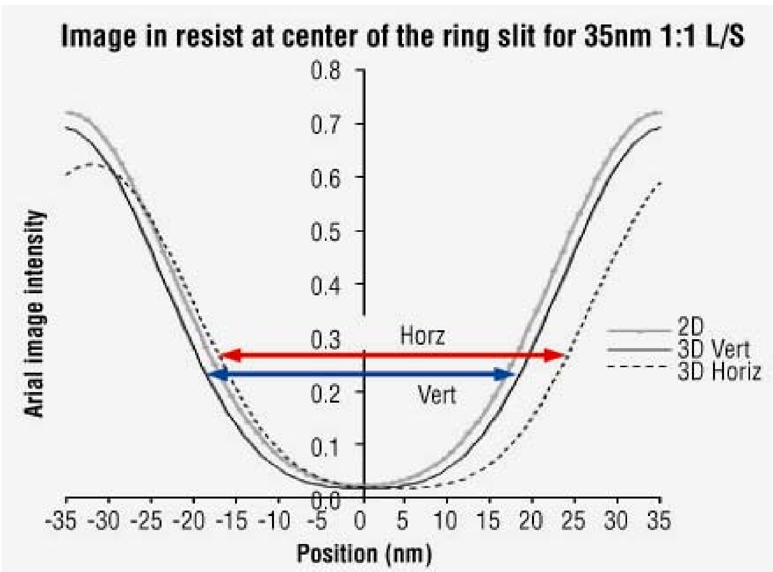
66° and 114° – at both edges of the ring field



Feature type	Orientation	Nominal CD, nm	Incident angle θ	Meas CD, nm
dense	vertical	35	90°	35.00
			66°, 114°	35.58
	horizontal	35	90°	36.89
			66°, 114°	36.62
iso	vertical	35	90°	40.01
			66°, 114°	40.26
	horizontal	35	90°	42.12
			66°, 114°	41.76

P. Brooker et al., Synopsys, October, 2008

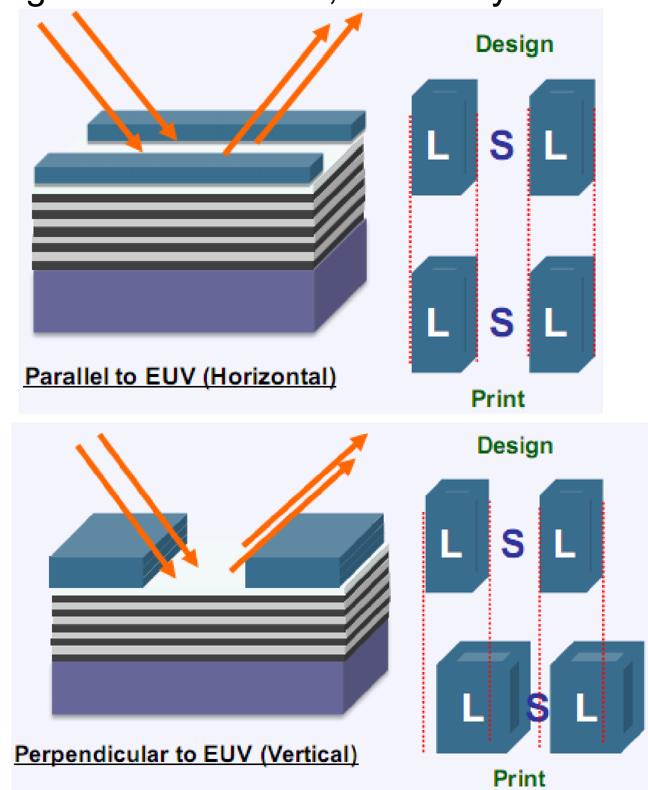
Image Shadowing due to 6° Illumination on thick EUV mask → Different 1D H-V Image Shift Across the Exposure Slit



Different 1D H-V image shift due to shadowing even at the center of the scanning slit

P. Brooker et al., Synopsys, October, 2008

The illumination beam is shadowed by the edge of the absorber, differently in H & V

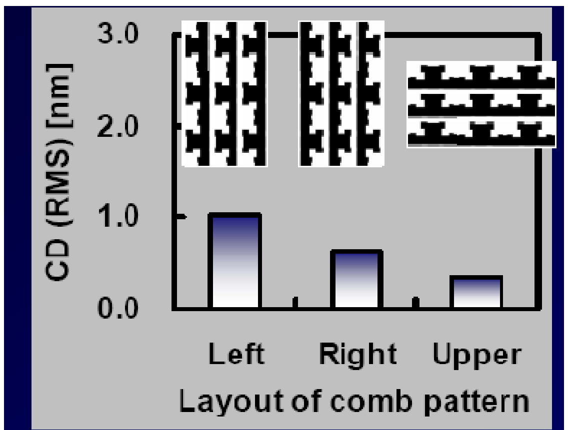


J. Ahn, Hanyang University, July 2009

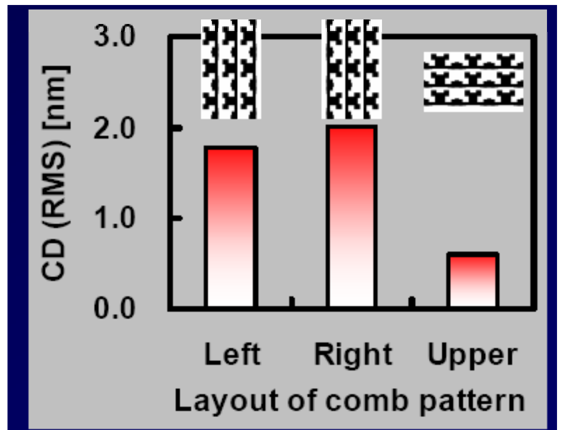
Image Shadowing due to 6° Illumination on "thick" EUV mask

Full-chip OPC is necessary for EUV

Mask shadowing causes more 2-D distortion at lower k_1



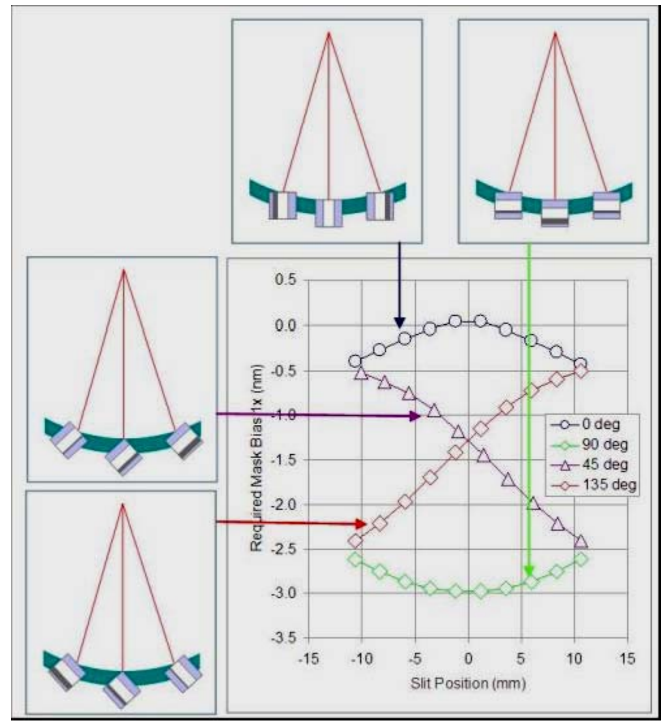
CD error in k_1 0.61 (33 nm dense)



CD error in k_1 0.41 (22 nm dense)

M. Sugawara, SONY, IEEE Litho Sym., Dec 2007

Across exposure slit – Different CD biasing necessary for different feature orientation.



http://www.imec.be/wwwinter/mediacenter/en/SR2006/681407.html

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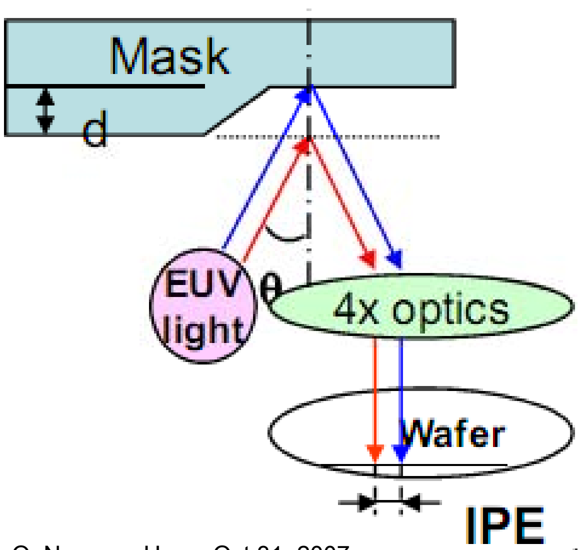
EUV Mask Blank Flatness Needs to be <50nm on Both Sides over 142mm^2 of 4X Field Area

EUV optics is non-telecentric at reticle plane

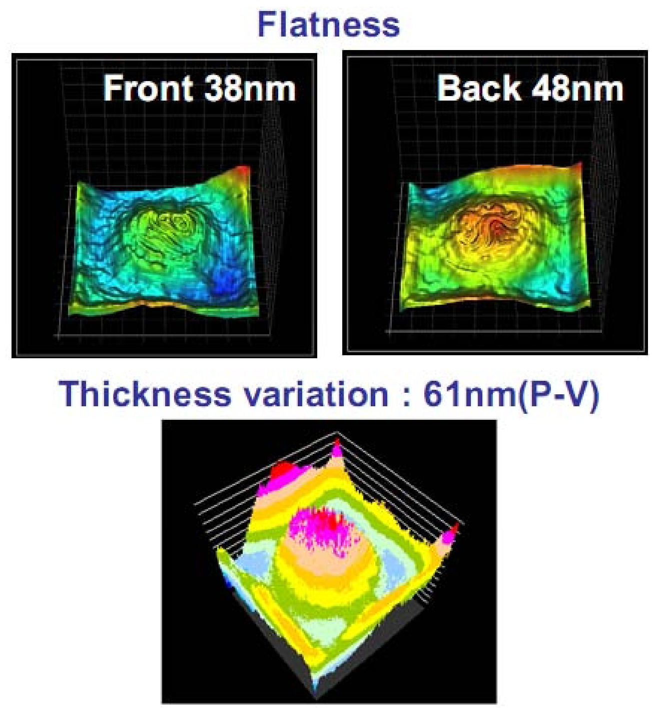
→ Very tight spec for mask blank flatness

→ Peak-to-Valley flatness variation causes image plane error on wafer

Desired 4X EUV mask blank flatness specification is <50nm for 22nm node



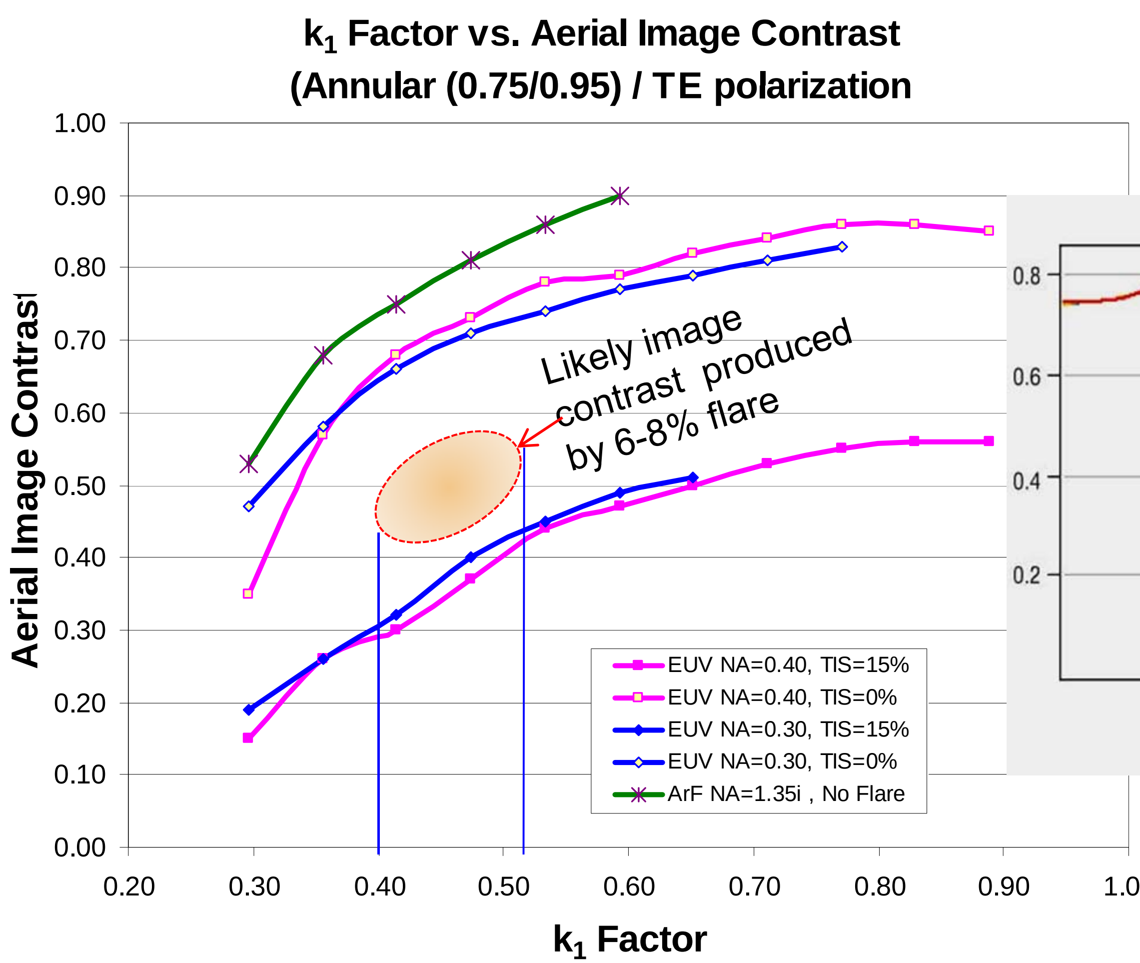
O. Nozawa, Hoya, Oct 31, 2007

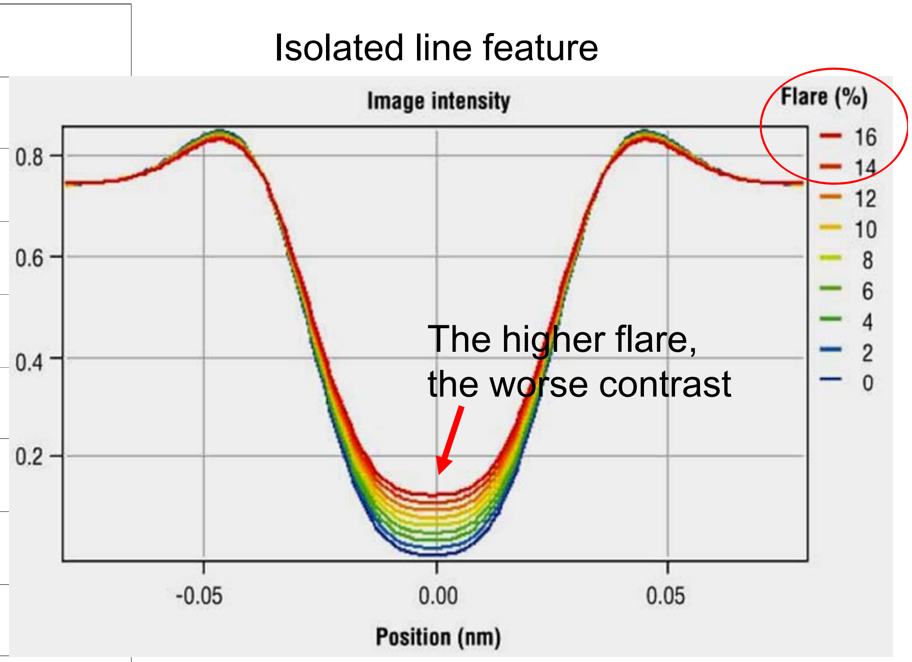


K. Okamura , Asahi Glass Co. Ltd, October, 2007

Flare reduces EUV aerial image contrast

EUV aerial image contrast (with 6-8% flare best achievable for production system) is worse than ArFi at the same k_1, OPC is likely needed





陳正方
J. Fung Chen

Why Does EUV Have So Much More Flare?

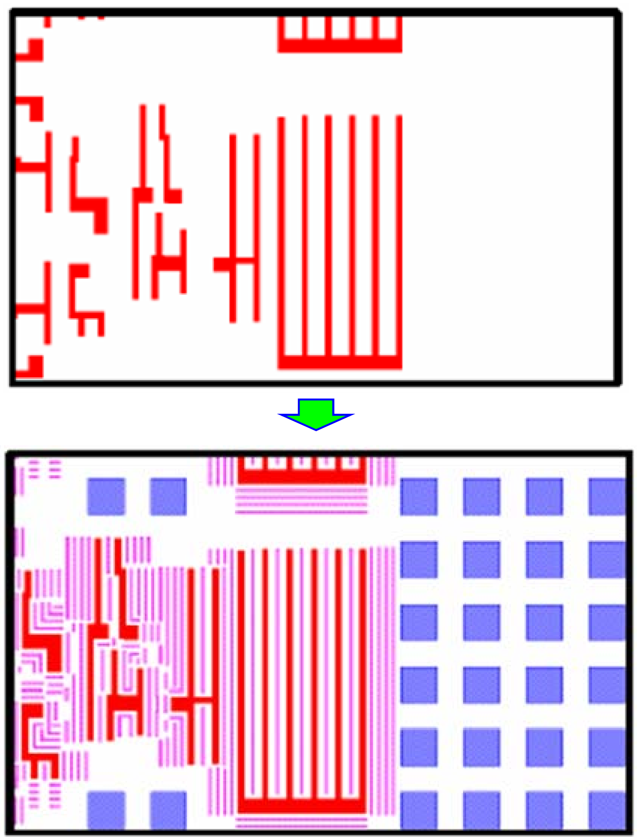
- Random light scattering from surface roughness of mirror (or lens) causes flare.
- Scattering in an optical system can be expressed as total integrate scattering (TIS). (Gullikson et. al., SPIE 1999). The bigger TIS, the worse flare.
- $$TIS = 4\pi^2 \left(\frac{rms_{phase}}{\lambda} \right)^2$$
- TIS is inversely related to wavelength (λ) to the power of 2. From 193nm to 13.5nm, TIS becomes ~100 times bigger and worse just due to wavelength reduction!
- TIS also relates to the square of surface roughness in terms of rms (root-mean-square) phase error. For EUV mirror system, due to reflection, inherently it has 2 times higher rms phase error.
- For ArF refractory lens, the two-sided surfaces are independent. Following the optical path direction, one surface side is in air and the corresponding side of the lens surface is in glass. The quadratic sum of rms phase error for every lens component becomes ~0.7rms.
- Comparing EUV to ArF system with the same surface roughness in a lens component, the TIS for EUV is about $(2/0.7)^2$, or roughly 10 times bigger and worse.

DFM for EUV Full-Chip Is Necessary

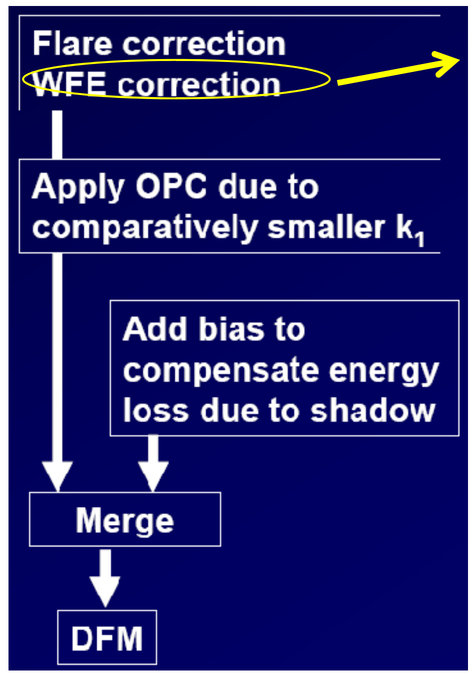
→ Pattern density compensation for <u>long range flare</u>

→ Non-telecentric imaging CD biasing due to mask feature shadowing

→ OPC for EUV low k_1 imaging

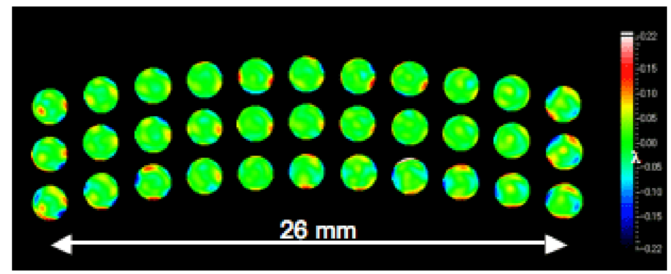


Schellenberg et al, Mentor SPIE 2005,



M. Sugawara et al., Japan, J. Appl. Phys, 46 (2007) 6554.

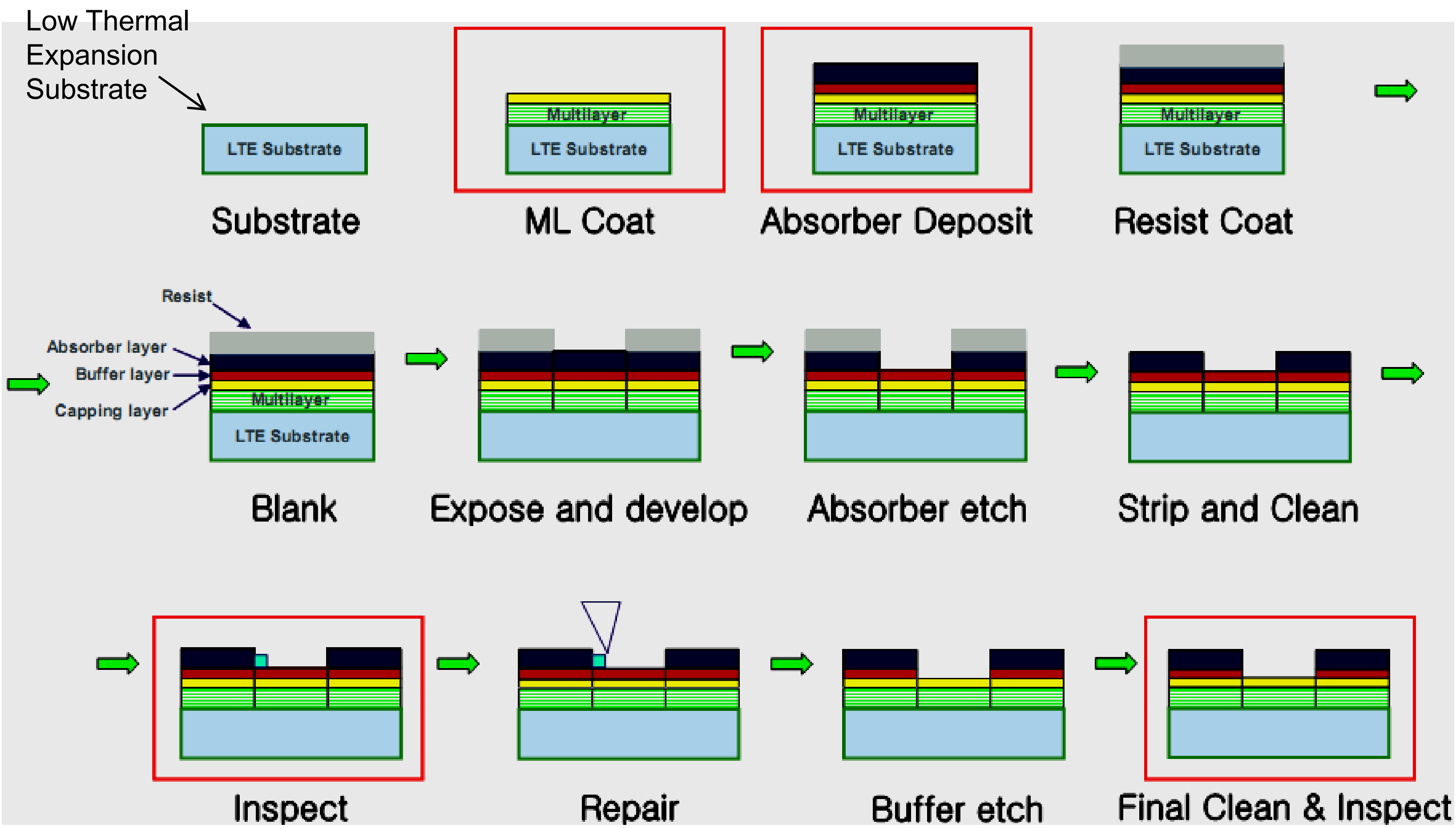
Extremely Small WFE (wave front error) Below 1nm RMS was Achieved in the Ring Field by Nikon



WFE 0.6 nm RMS (average)
Max. 0.8 nm RMS ~ Min. 0.3 nm RMS

http://www.nikonprecision.com/newsletter/summer_2008/article_03.html

EUV Reticle (Mask) Making Process



S. Watson, KLA-Tencor, July 2, 2009

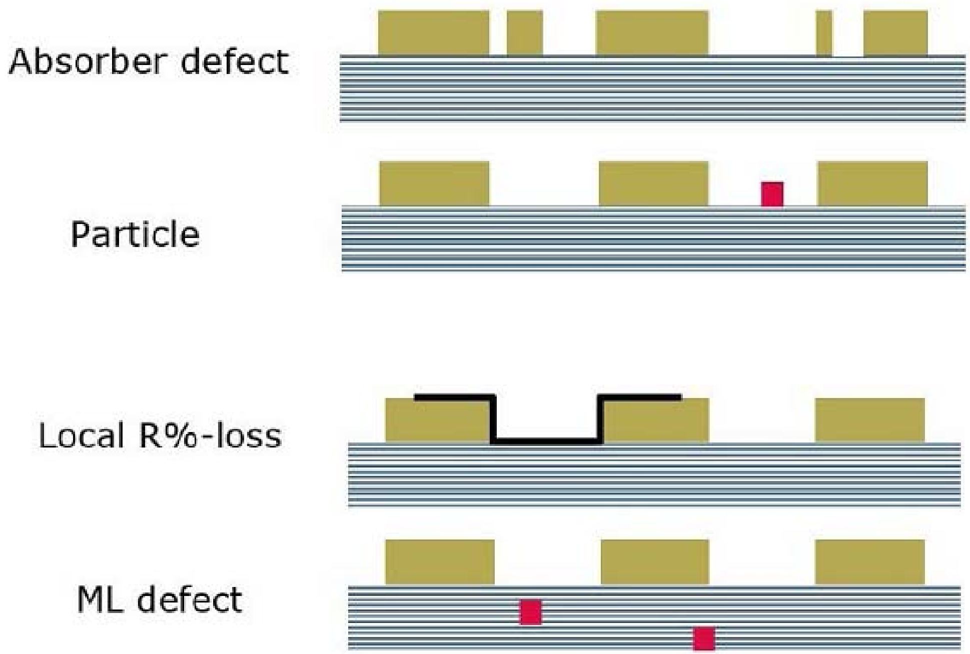
Four Types of EUV Mask Defects

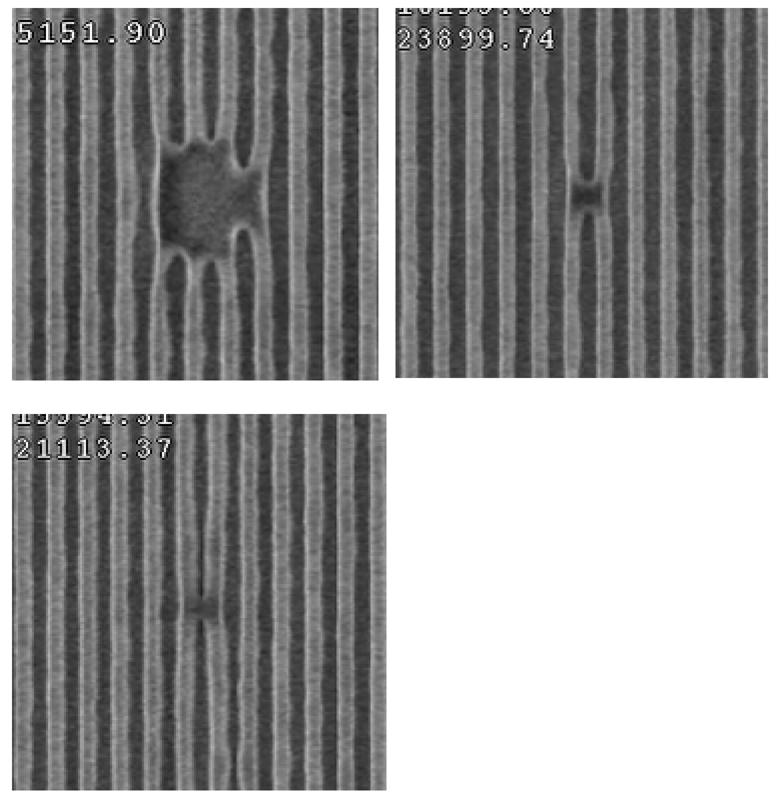
Current Status on Mask Defectivity is < 0.2/cm^2 (80 nm Reticle Sensitivity)

Production Target (with 25 nm Reticle Sensitivity)

< 0.003/cm^2 for Logic

< 1.0/cm^2 for Memory

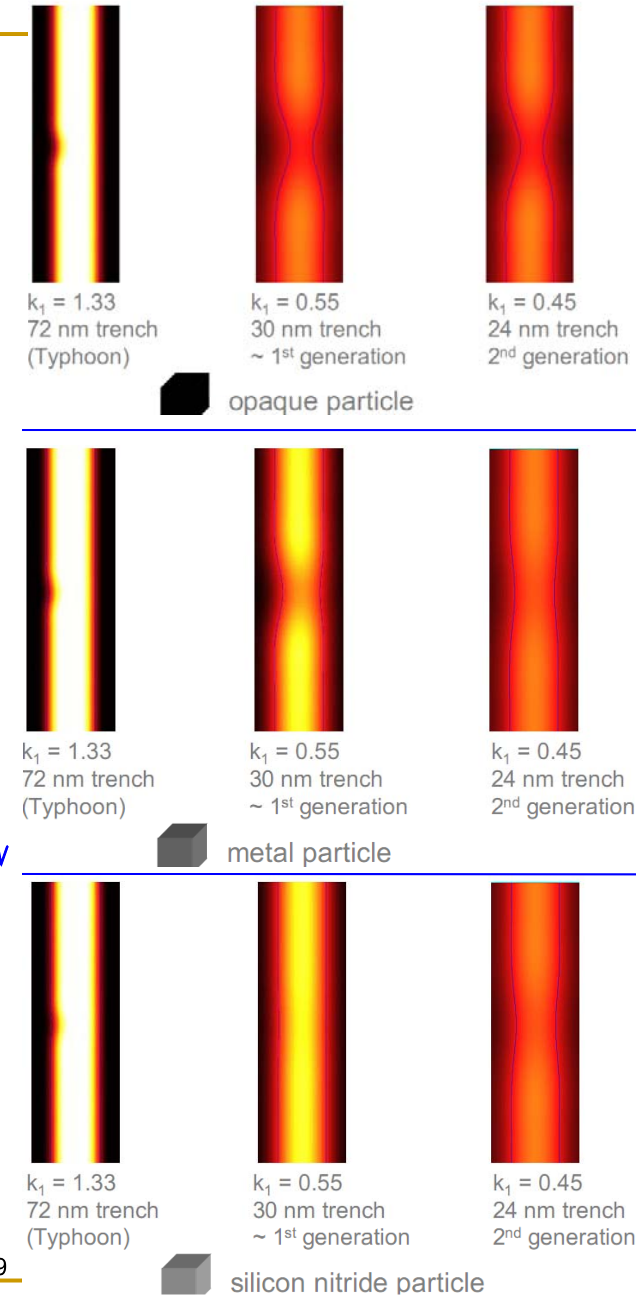




S. Watson, KLA-Tencor, July 2, 2009

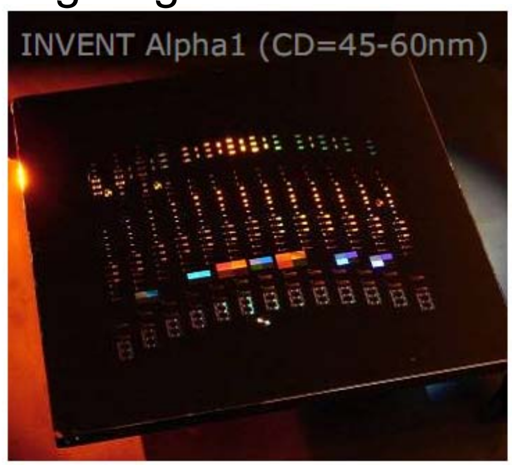
EUV Mask Defect Printability Depends on the types of debris and k_1

Three types of 50nm defect on imaging at NA=0.25



Mask defect printability less forgiving at smaller CD

Only ~1-3% of blank defects found to be printable on wafer



~10% of blank defects found to be printable on wafer

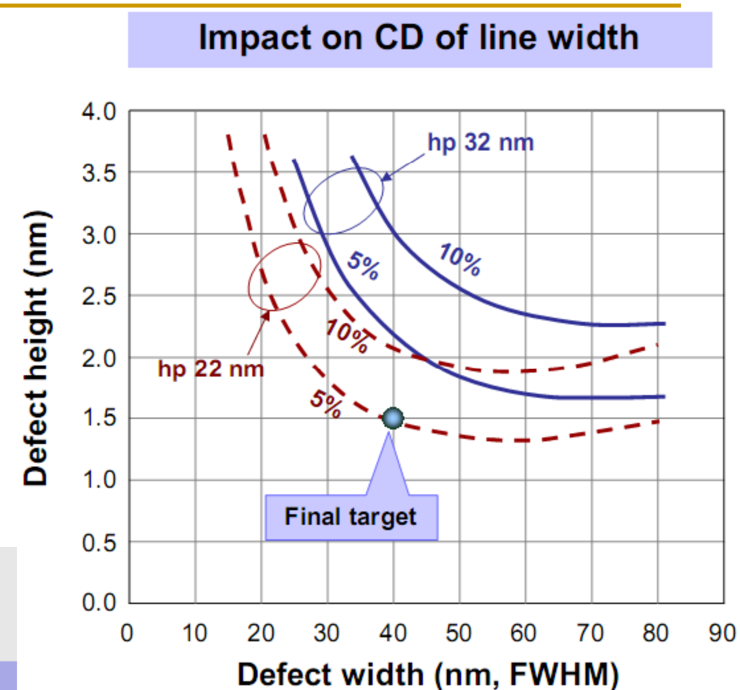
B. La Fontaine, Global Foundries, July 15, 2009

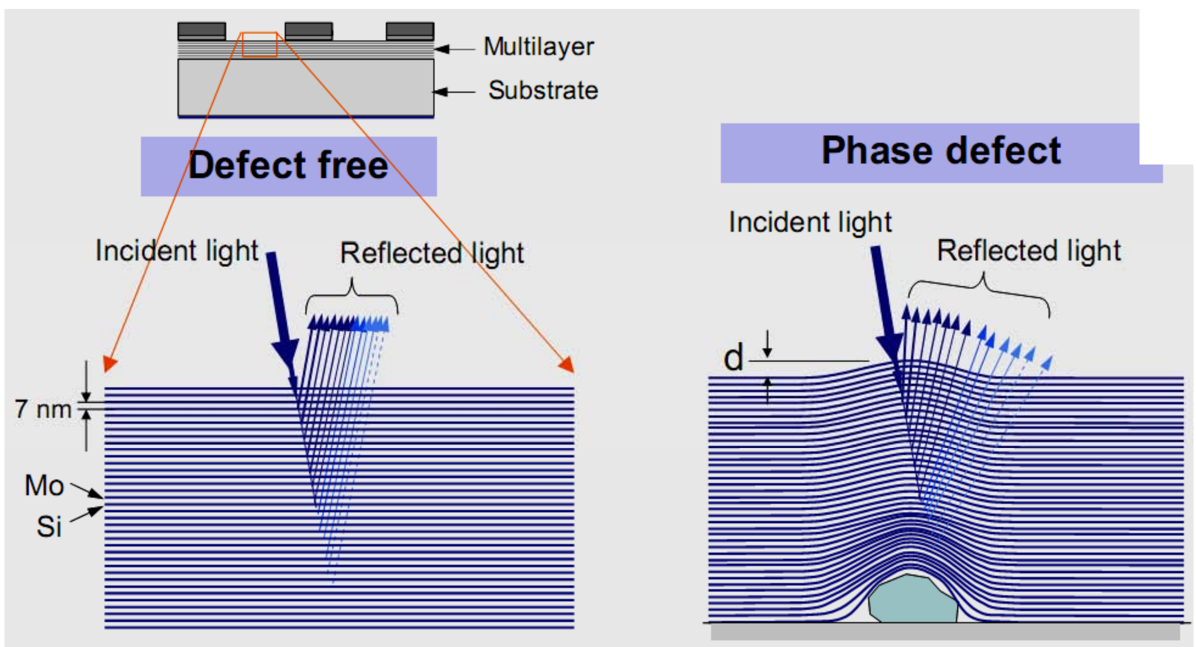
EUV Mask Blank "Phase" Defects → CD Variation

For 22nm HP, 4X EUV mask blank defect to cause <5% CD variation –

→ FWHM defect size < 40nm (4X mask)

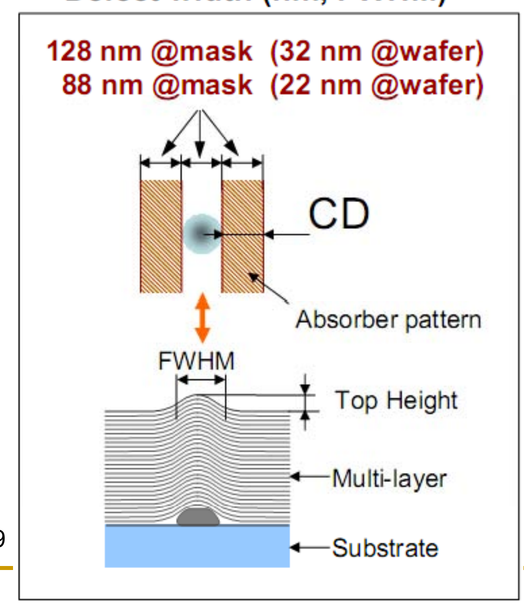
→ defect height < 1.5nm (4x mask)



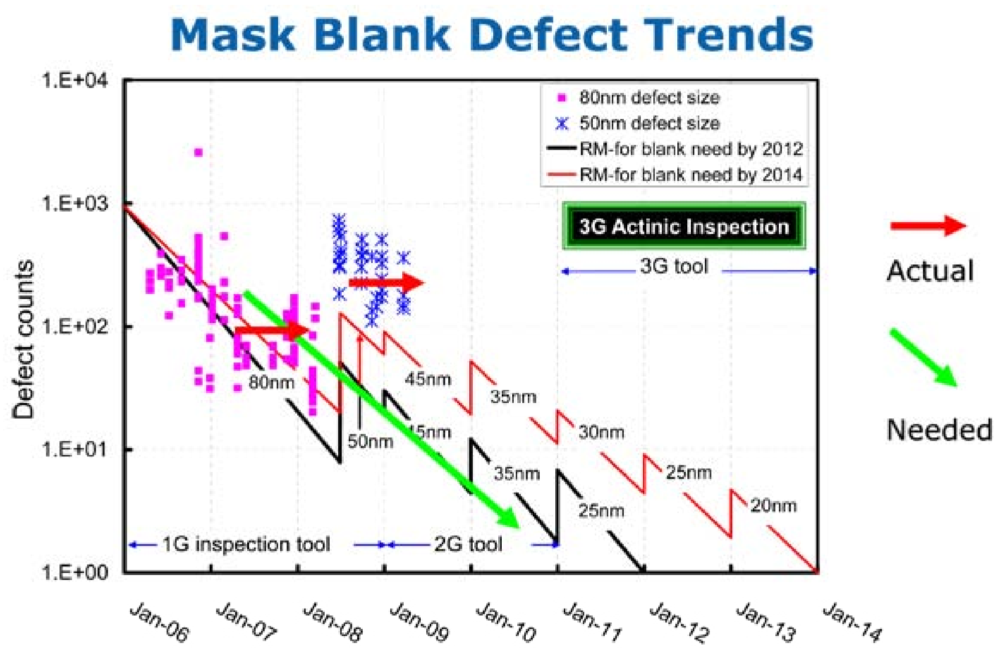


Bump or pit of multilayer results in a phase defect

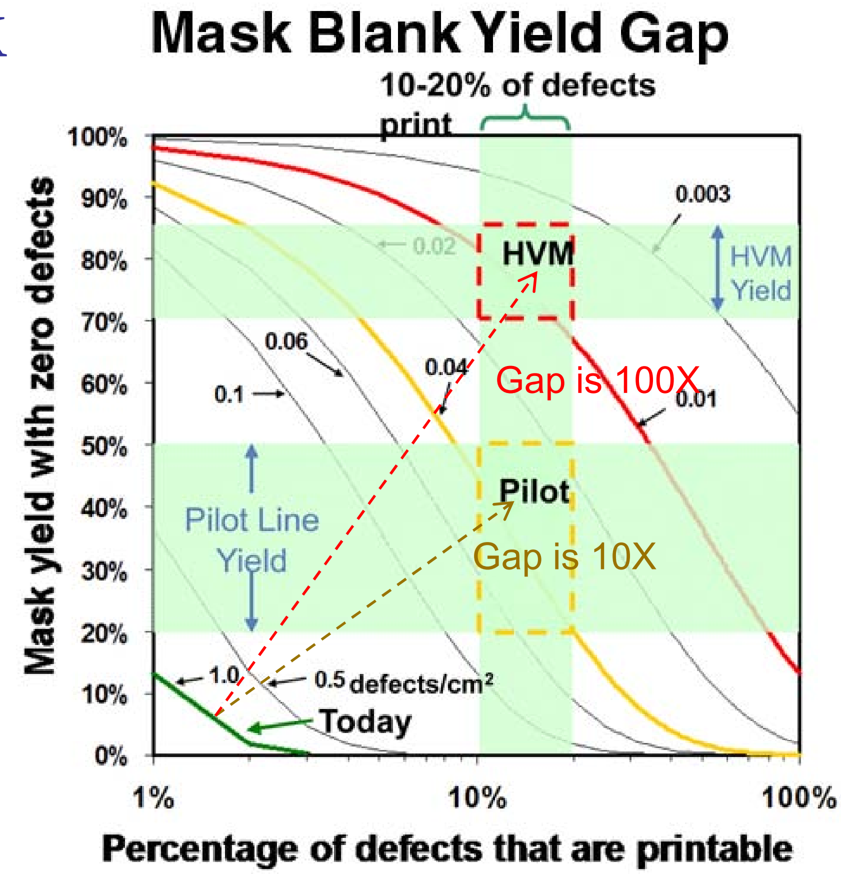
T. Terasawa et al., Selete, June, 2009



EUV source for mask blank defect inspection is the top concern for HVM



The metrology tool gap is considered one of the biggest threats to high-volume EUV lithography insertion. (Intel, July 2009)

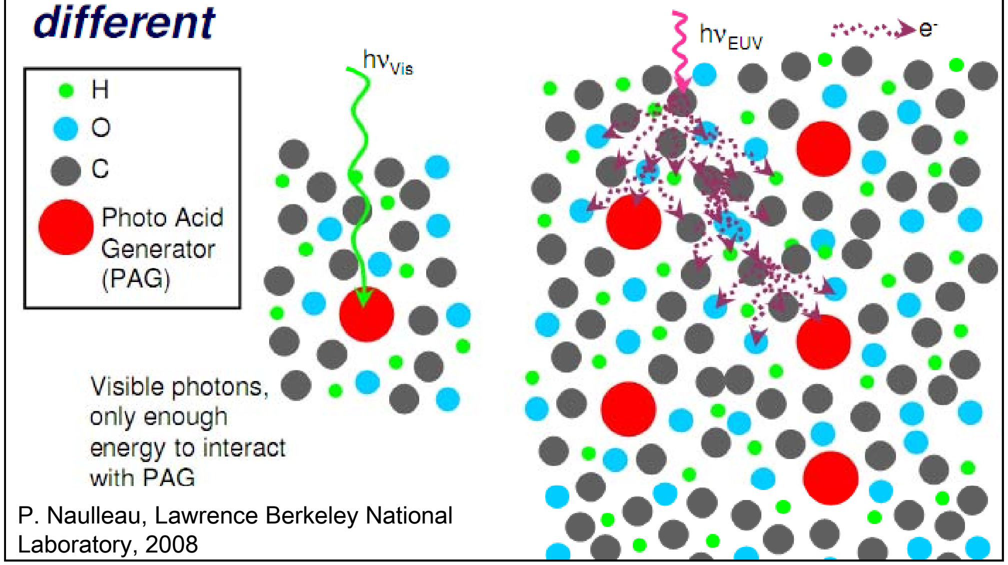


Although the historical "defect-free" target for EUV mask blanks is 0.003 defects/cm2 at 18 nm, recent data suggests only 10-20% of defects print. The ultimate HVM defect density target might be 0.01 defects/cm2 at 18 nm. Today's level is 1 defect/cm2 at 18 nm. (Intel, July 2009, w/ data from Sematech)

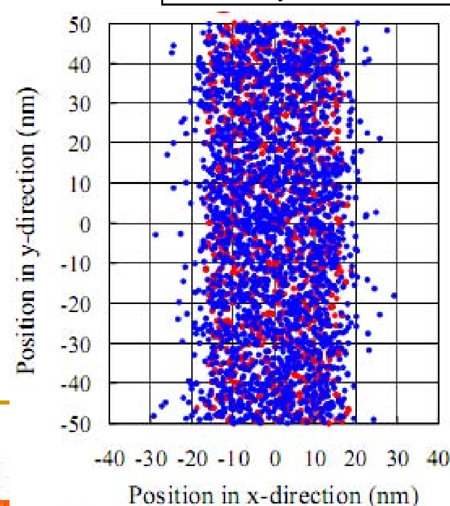
EUV Imaging with Chemically Amplified Resist (CAR)

- EUV energy (92 eV) >>> activation energy of Photo Acid Generator (PAG)
- EUV photons interact with all atoms, not just PAG
- EUV photons do not directly activate PAG
- But rather generate secondary electrons upon interaction with first encountered atom
- Secondary electrons eventually activate PAG

Although most EUV resists are based on 193 or 248 nm systems, EUV interaction with resist these materials is fundamentally different



P. Naulleau, Lawrence Berkeley National Laboratory, 2008



Proton-anion distribution

For EUV exposure:

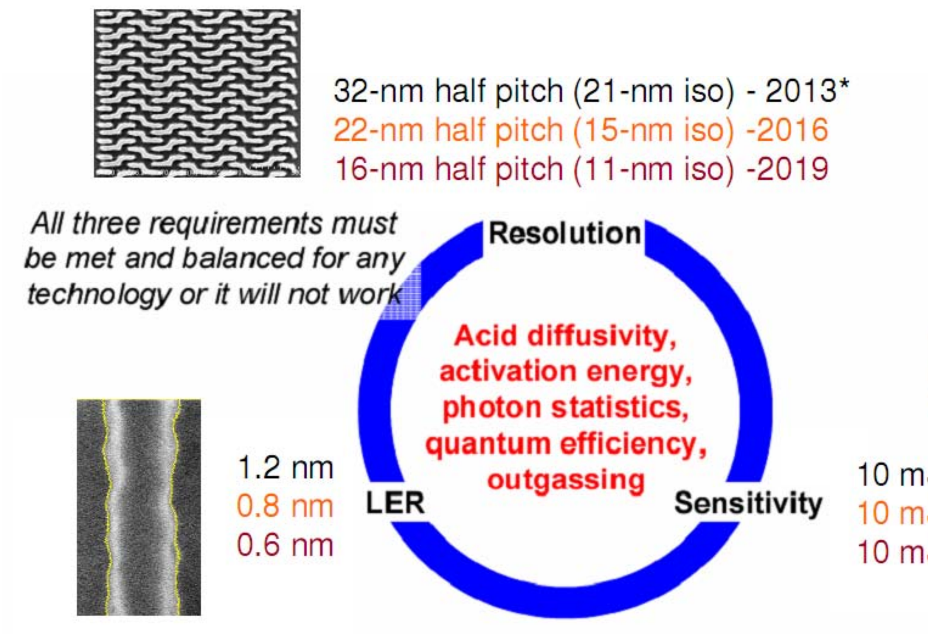
1) Accumulated energy profile (red) ≠ Latent acid image (blue)
2) Big impact on sensitivity, resolution and LER

T. Kozawa et al., Osaka University, July, 2009

EUV Resist 3-Way Trade-offs

LER reduction is the most serious problem!

Simultaneously meeting resolution, sensitivity, and LER crucial issue for EUV resists



LER: Line Edge Roughness

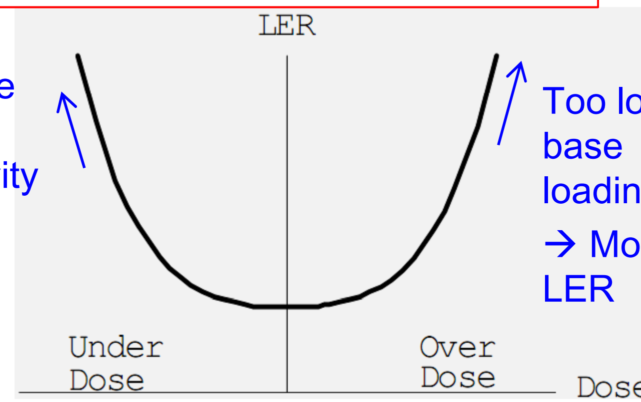
* 2007 ITRS Roadmap

P. Naulleau, Center for X-ray Optics, Lawrence Berkeley National Laboratory, 2008

$$\sigma_{LER}^2 \times dose \times blur \simeq \text{constant}$$

Increase base loading for more sensitivity

→ More LER



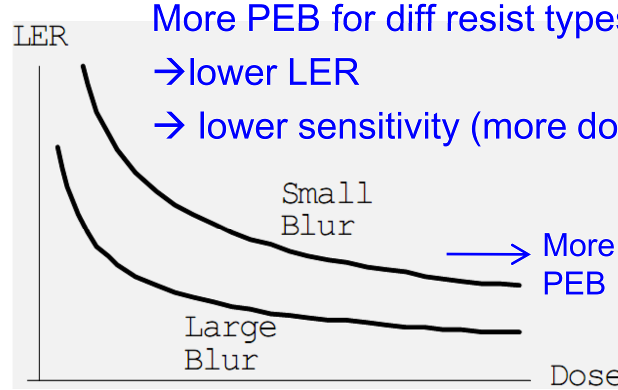
Too low base loading

→ More LER

More PEB for diff resist types

→lower LER

→ lower sensitivity (more dose)



More PEB

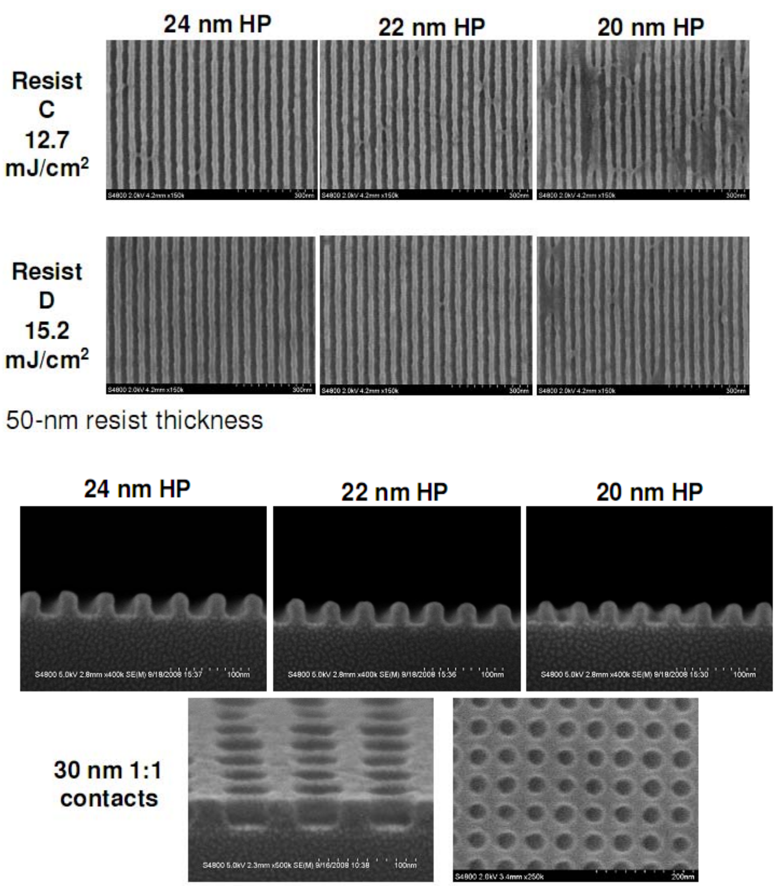
LER for 193 nm resists is more a process related effect.

But for EUV, LER is enhanced by shot noise or photon counting effects.

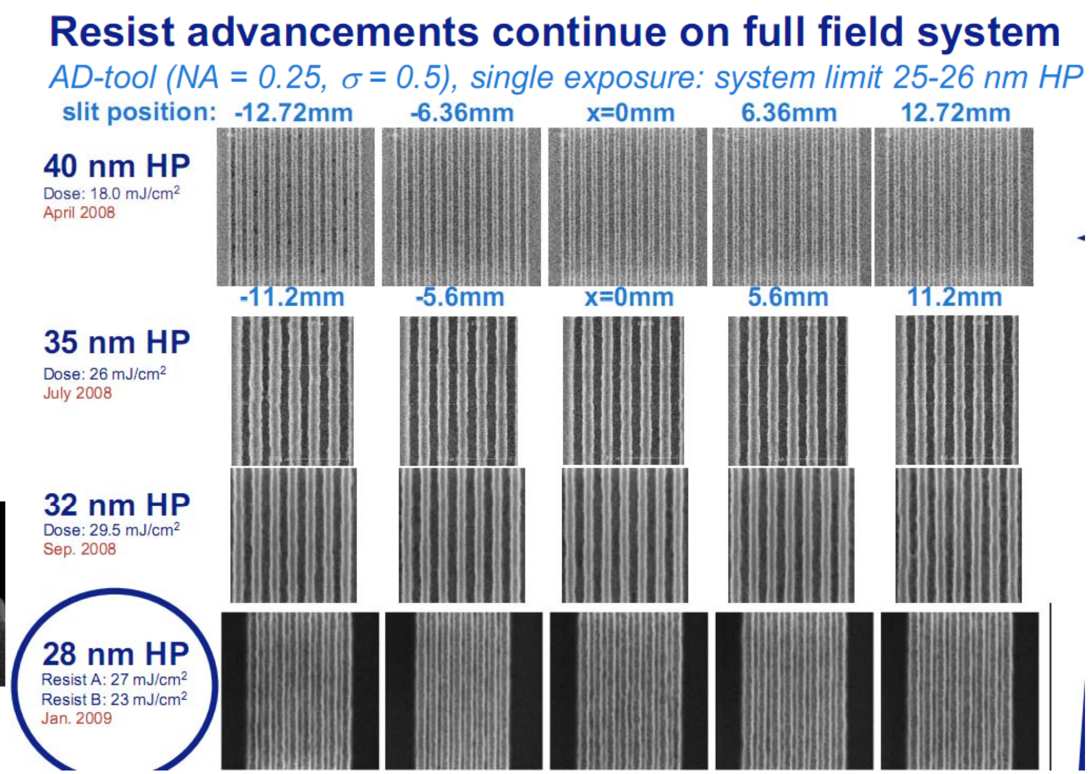
JM Hutchinson, Intel, 1998 SPIE

G. M. Gallatin, IBM T. J. Watson Research Center, 2005 SPIE

EUV Resist Resolution Is Progressing …



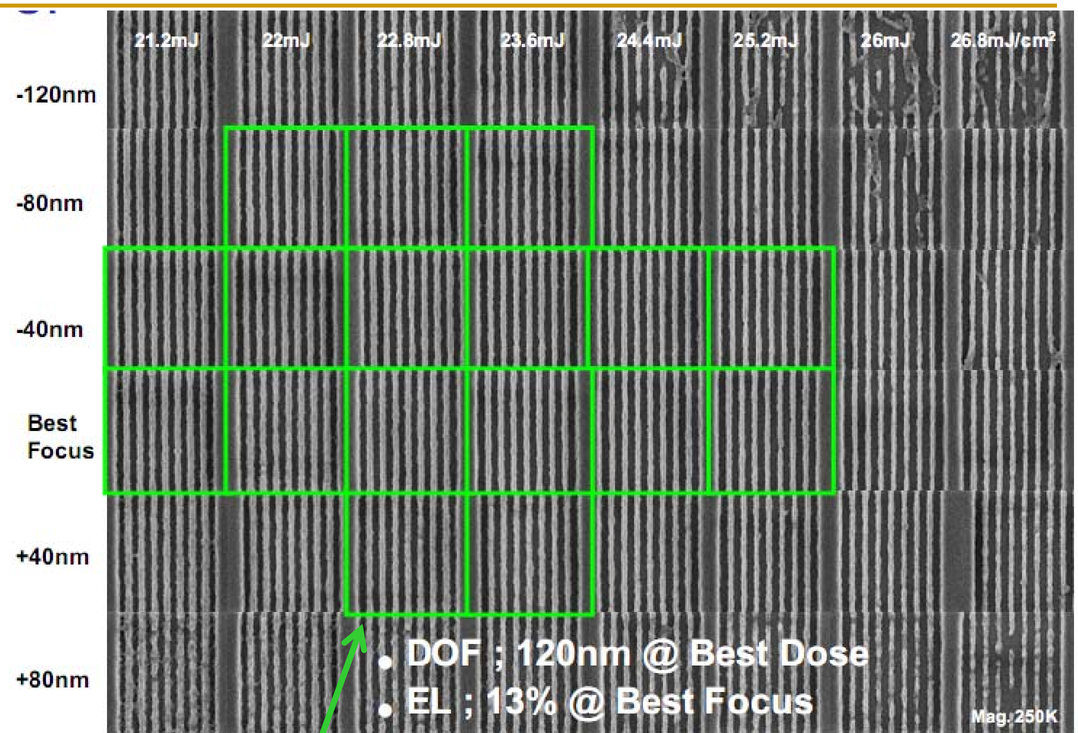
Resist D, film thickness = 50 nm



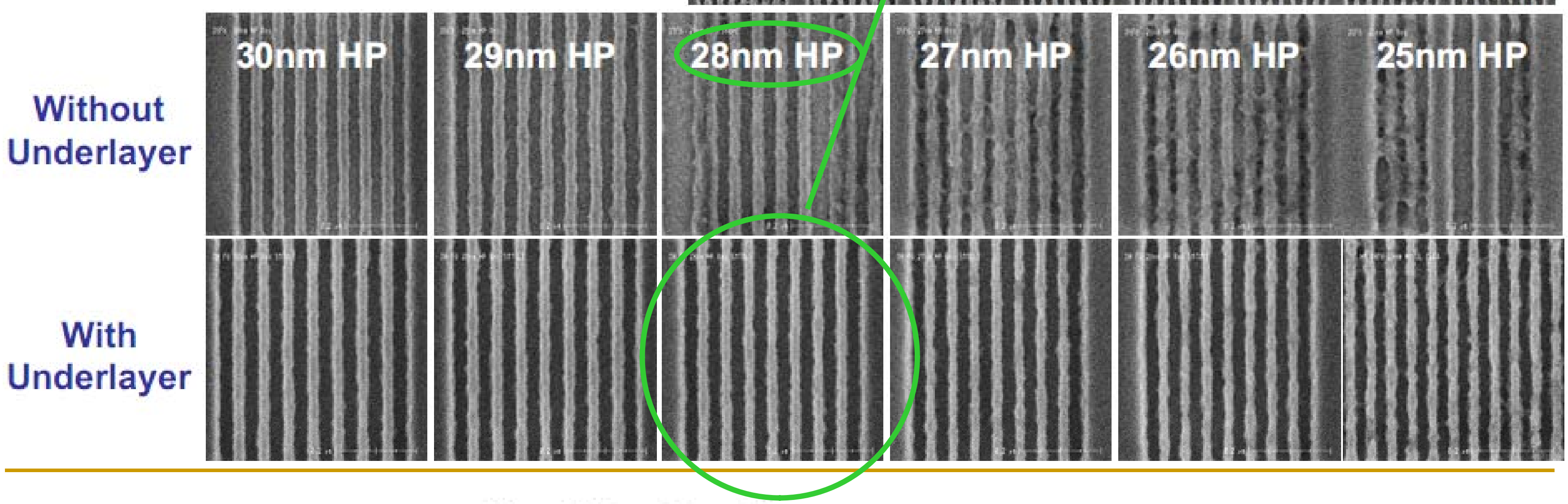
ASML, SPIE, 2009

State-of-the-Art EUV Resist Process → 28nm HP with 5~6nm LER

(SEMATECH, Sept 2009)



Line Edge Roughness (LER)
→ Line Width Roughness (LWR)



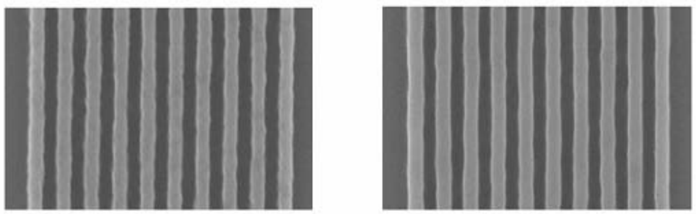
Reduce LER by Rinse Agent after Resist Develop

Rinse agents for LER reduction without resolution or sensitivity trade-offs

Berkeley MET

XP5494-C resist,

Y-M

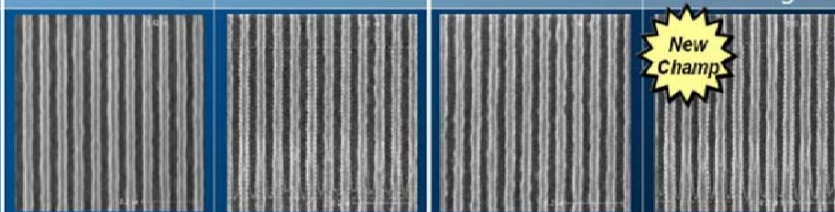


Baseline Process	Rinse Agent Process
CD = 41.7 +/- 0.8 nm LER = 4.3 +/- 0.4 nm	CD = 40.6 +/- 0.6 nm LER = 3.2 +/- 0.4 nm

- Rinse agent applied instead of water after develo
- ~1-nm reduction in LER observed
- No effect on resolution or sensitivity

Data courtesy of Tom Wallow, AMD

Rinse Agent Improves EUVL Manufacturability

30 nm HP	1H'08 "Smooth" RLS Champs		"Fast" RLS Champion	
	Resist A	Resist B	Resist C	Resist C + Rinse Agent
				
MIN LWR (nm)	3.8	4.3	5.3 → 26%↓ →	3.9
DOSE (mJ/ cm²)	14.0	11.0	8.7 → 38%↓ →	8.7
Z-Factor[1]	2.2 E-08	2.4 E-08	3.3 E-08	1.8 E-08

[1]Wallow, et al SPIE 69211F (2008)

- **Pre- and/or post-processing techniques can significantly improve roughness of high resolution / fast EUV resist.**
- **Focus on continued material evolution for improved pattering and LER/ LWR reduction.**

intel

Lithography Cost Of Ownership for 22nm HP

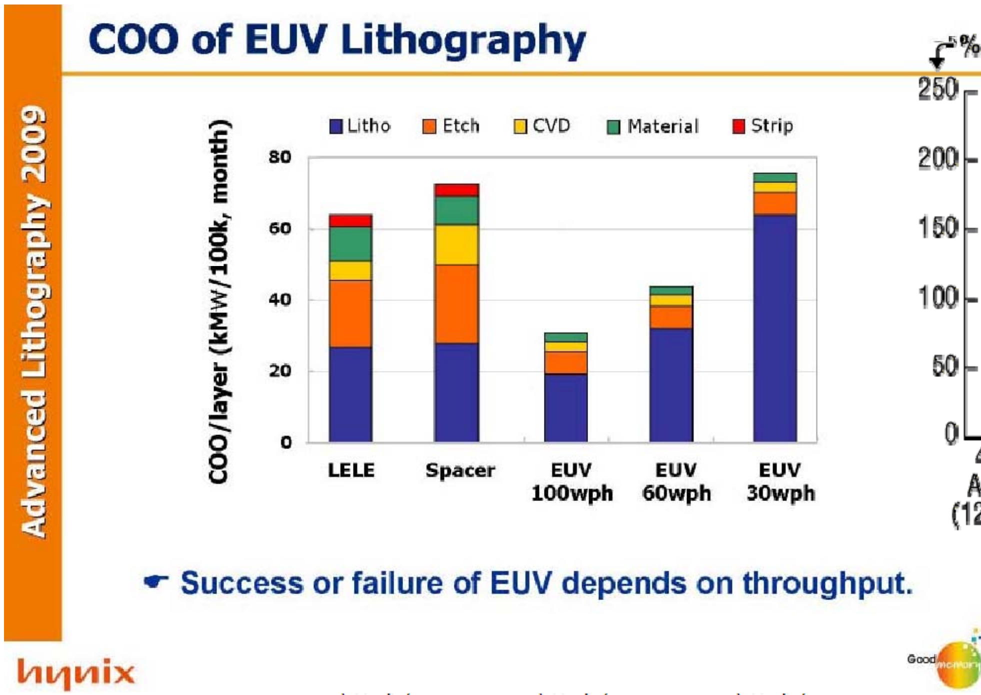
NAND manufacturing likely to be the first to adopt EUV

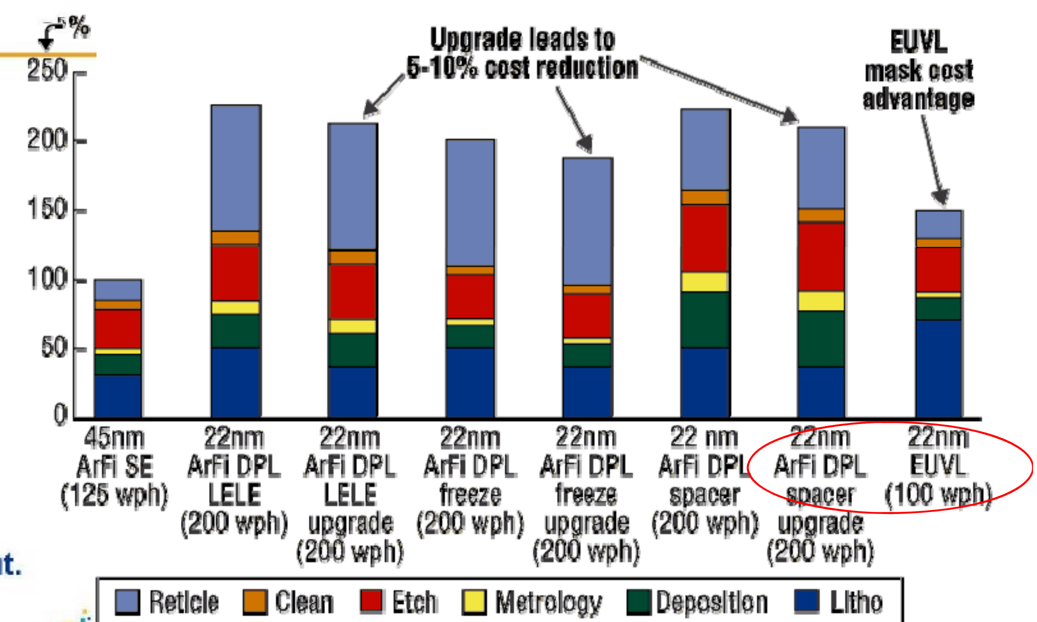
→ COO comparison (DP vs. EUV) can be useful for NAND

But, for foundry –

→ <u>EUV mask infrastructure must be ready due to too many mask sets</u>

→ <u>EUV full-chip OPC can be overwhelming for foundry computational capacity</u>





A.Wüest, Sematech, 2009 SPIE

EUV Infrastructure Gaps

SEMATECH

Gap	Suppliers Building Solution?	Estimated Cost for HVM Solution	Time to HVM Solution
Full Field Production Scanner	Yes (2)	Funded	2012
Source	Yes (3)	Funded	2011
Resist	Yes (Many)	Funded	2011
Mask Substrate	Yes (2)	Funded	See Below
Optical Inspection	Yes (1)	Funded by SEMATECH	2011
Mask Blank	Yes (2)	Funded	See Below
Multilayer Deposition	Yes (1)	Funded by SEMATECH	2011
Actinic Inspection	No	> $50M	2013?
Defect Review	No	> $50M	2013?
Mask: Patterned Inspection	No	> $100M	2013?

- EUV's key infrastructure gaps are in the area of mask metrology

Bryan J. Rice, SEMATECH, July 15, 2009

Outline

- Lithography Manufacturing beyond 22nm
  - ArFi Double Patterning (DP)
  - SMO and Contact Hole Imaging
  - EUV
- Alternative Lithography Manufacturing
  - Massively Parallel e-Beam
  - Nanoimprint
  - Through Silicon Vias (TSV)
- Moore's Law & Lithography Manufacturing Roadmap

Alternative Lithography Manufacturing – better IC density but concerns on cost

- Massively Parallel e-beam Direct Write
  - Throughput, throughput, throughput
    - Data transfer throughput
    - Beam current requirement for throughput
- Nanoimprint
  - Capable of very high resolution
  - 1X master mask quartz defect is very hard to avoid
- Through Silicon Via (TSV) for 3D IC
  - TSV to increase IC density
  - Via first vs. Via last

Mapper Massively Parallel e-Beam

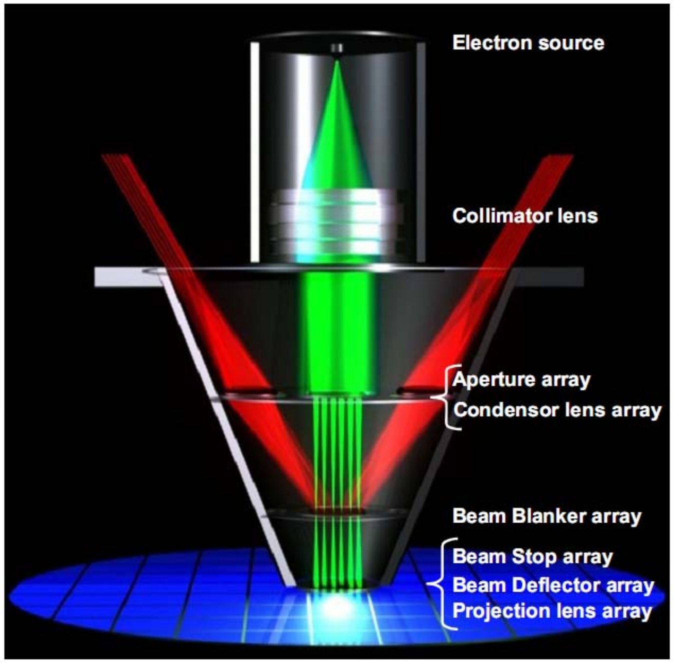
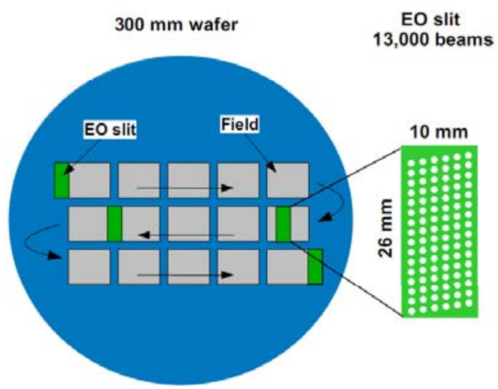


Table 1 Exposure analysis results

Pattern	CD [nm]		CD Mean -to-target [nm]	CDu [nm]
	Measured	Target	Measured	Measured
Dots dense	43.4	45.0	1.6	2.5
Horizontal dense	42.8	45.0	2.2	1.9
Verlines-dense	44.9	45.0	0.1	2.8

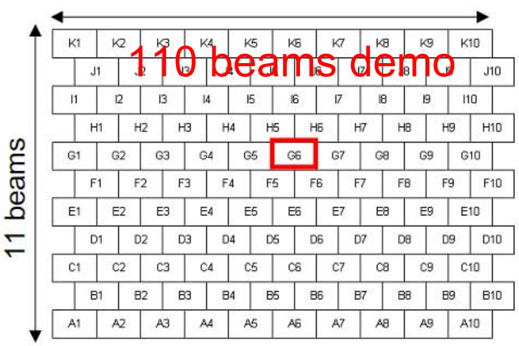


One reality question to ask M. e-beam supplier:

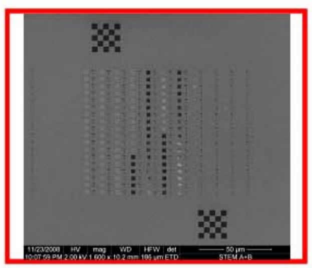
How much total beam current can you do today?

Throughput Calculations:

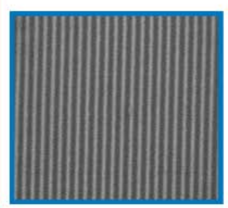
1) Resist exp → 30 μC/cm²
2) 15 WPH →150μA / wafer
3) 150μA =15nA/beam x 10000
4) 0.2μA to resolve 45nm CD
5) 5KV for 8nm overlay
6) 7.5GHz/channel data rate



Exposure area of 110 beams: 1.4 mm x 1.5 mm



Exposure area of 1 beam: 130 μm x 150 μm

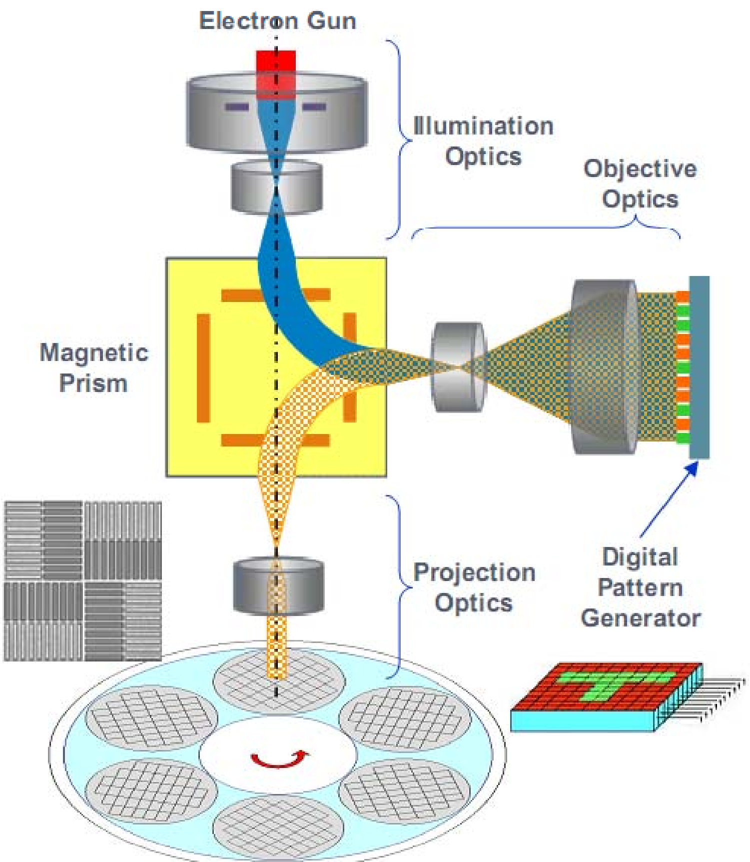


3 μm x 3 μm snapshot

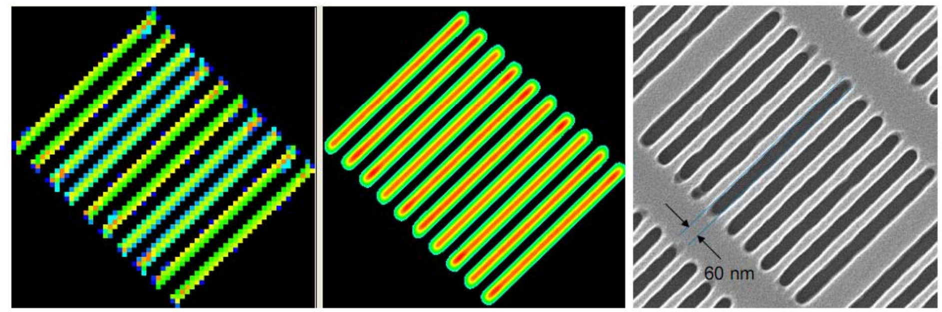
M. J. Wielan, et al., Mapper Lithography, 2009 SPIE

Reflective Electron Beam Lithography (REBL)

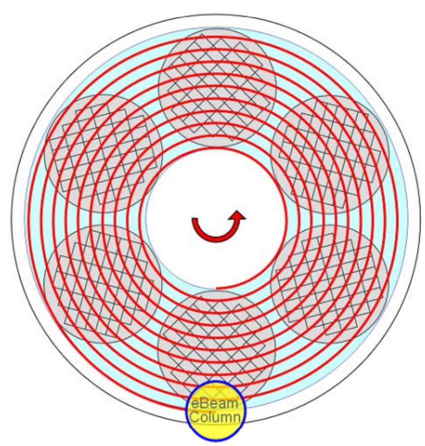
REBL Nanowriter Concept



TDI Integrated Dose showing Gray Level Pixel Dose | Beam Blur convolved with Integrated Pixel Dose | Emulated Writing Strategy using Vistec VB6 Ebeam Writer



Pixel Size = 24 nm Equal Lines & Spaces with 60 nm HP | Beam Blur = 32 nm Convolved with pixel dose | TDI Integrated Dose showing Gray Level Pixel Dose



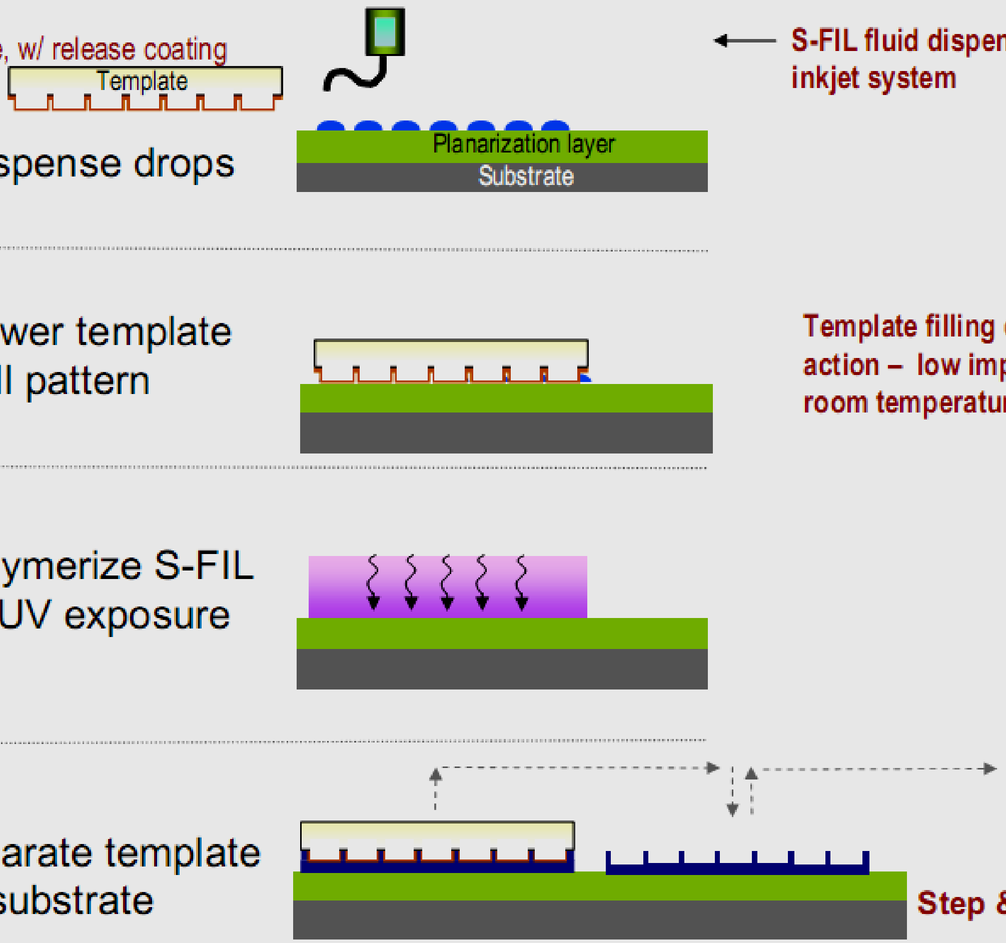
1. Reflective Optics
2. Massively parallel exposure (> 10^6 beams)
3. Targeting up to 10 wafers/hour (single column) with resolution of 45 nm, extendable to 32 nm and beyond

M. McCord et. al., KLA-Tencor, June 30, 2009

Step and Flash Imprint Lithography (S-FIL®)

transparent template, w/ release coating

S-FIL fluid dispense using inkjet system



Step 1: Dispense drops

Step 2: Lower template and fill pattern

Template filling driven by capillary action – low imprint pressure and room temperature process

Step 3: Polymerize S-FIL fluid with UV exposure

Step 4: Separate template from substrate

Step & Repeat or whole wafer imprint

S-FIL process diagram courtesy of Molecular Imprints, Inc.

2

陳正方
J. Fung Chen

Defect in the quartz mask template could be the killer for Nanoimprint→ Toshiba Study

Nanoimprint can apply for unit process study, and test device fabrication.

•As the result of basic evaluation,

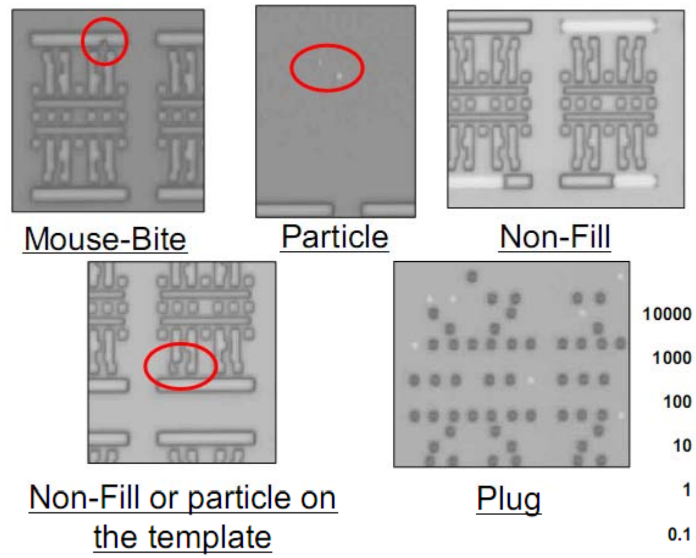
Item	Score	Comment
CD uniformity	☺	< 0.8nm
LER	☺	< 2nm
Overlay accuracy	☺	~20nm
RLT	☺	RLT mean ~15nm, variation ~4nm
Template resolution	☹	Under improvement by template vender
Defectivity	☹	DD < 10pcs./cm² Under improvement

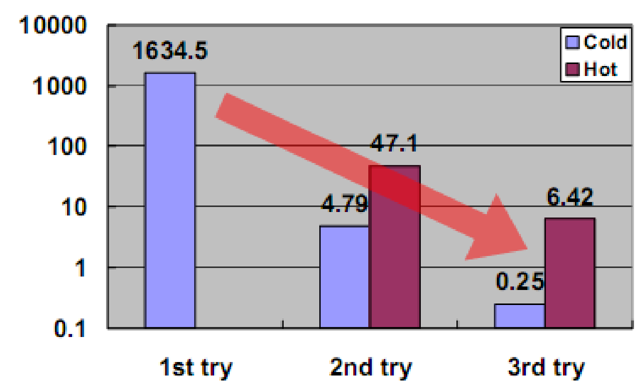
>> We hope the throughput will be slightly better.

•As the result of test device fabrication,

- ➢ 20nm trench is created.
- ➢ Overlay accuracy of test device is less than 11nm(M±3σ).

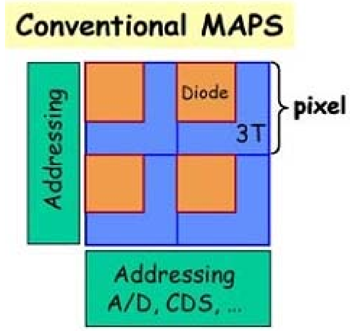
TOSHIBA Leading Innovation >>> T. Higashiki, Toshiba, December 2007 24

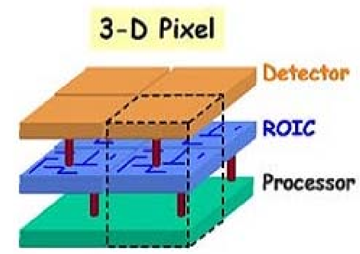


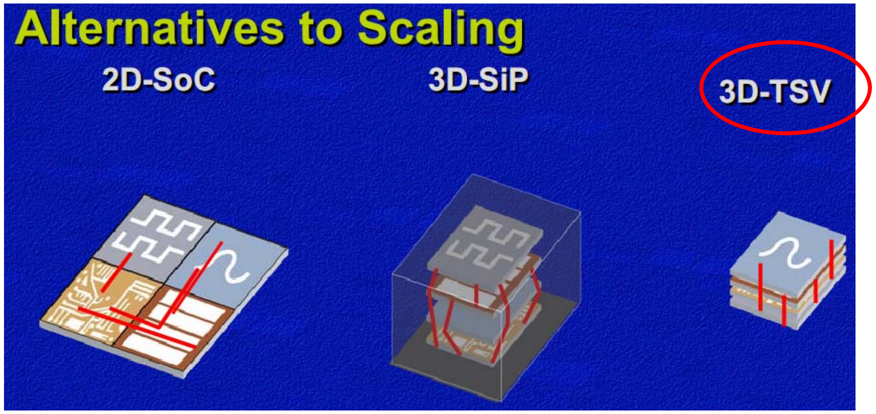


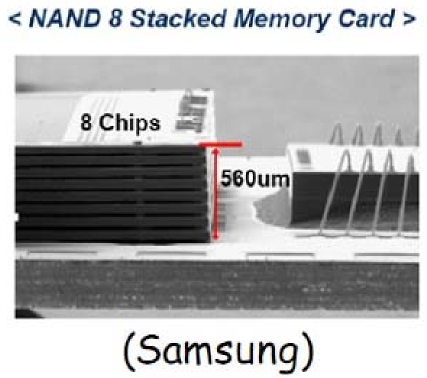
Through Silicon Vias (TSV) for 3D Integration

- Why the major pushes by the industry for 3D IC? → to increase circuit density!
  - Pixel arrays for imaging – current 2D approaches cannot handle the data rate needed for high speed
  - Memory – the cost of 3D can be much less than going to the next technology node.
- 3D integration increases chip density by combining multiple chips to together







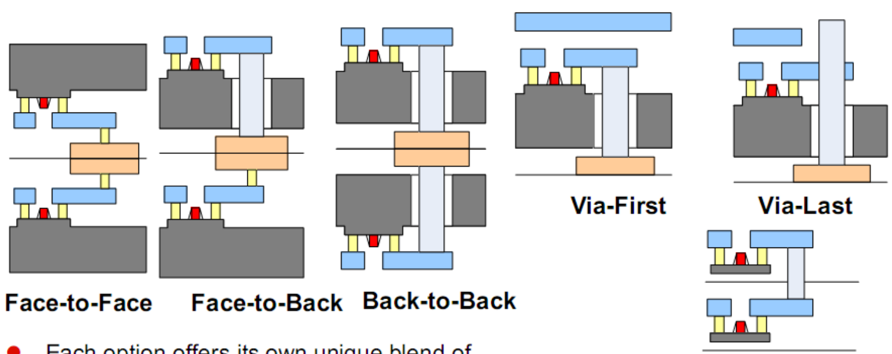


R. Yarema et al., MIT Fermilab Pixel Design Group, Sept, 2008

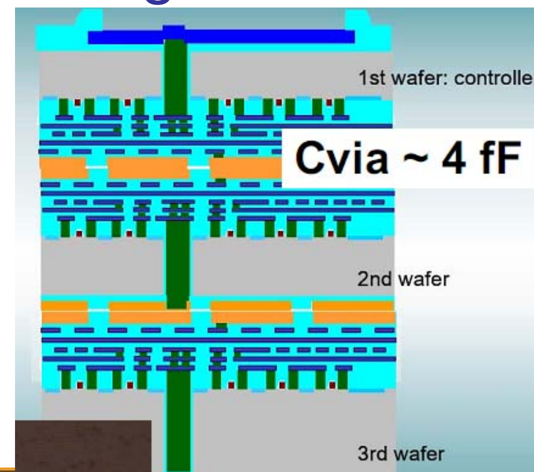
TSV Decreases Yield Risk –

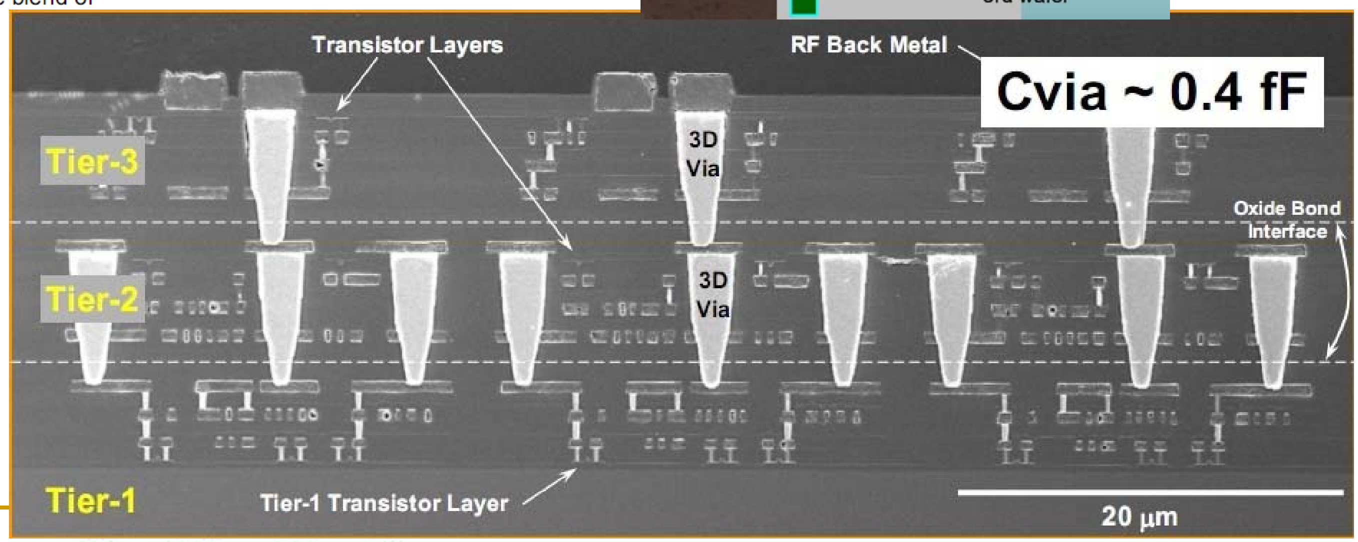
Stacking a 130 nm analog die with a 45 nm digital die, rather than trying to build a 45 nm mixed signal SOC

Transistor/TSV Integration Options



- Each option offers its own unique blend of
  - Cost
  - Via Density
  - Routing Congestion
  - Heat Dissipation





A 3D-specific memory-on-logic stack can reduce power by 50% while increasing performance

P. Franzon et al., NC State U, July 2009

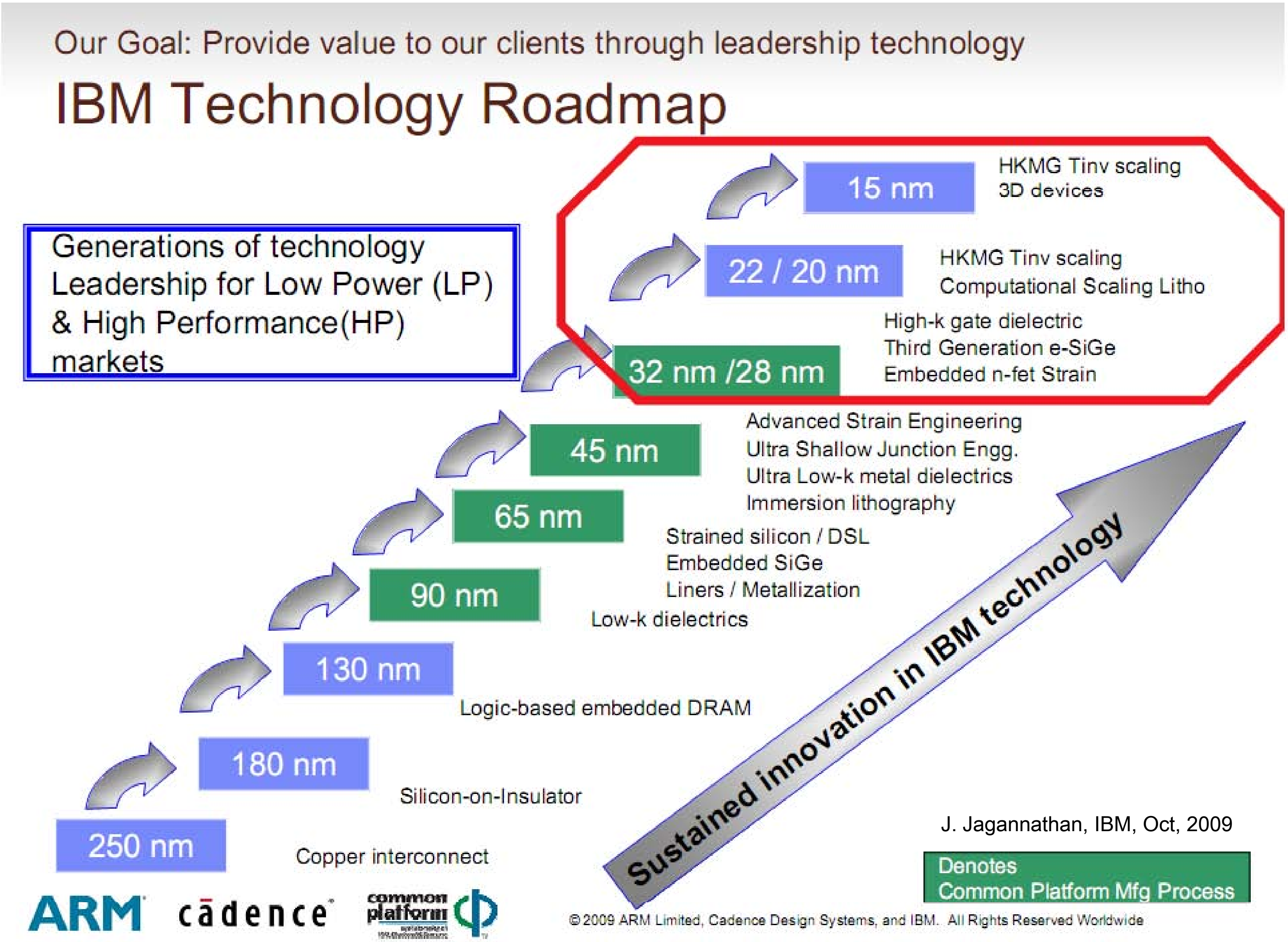
Outline

- Lithography Manufacturing beyond 22nm
  - ArFi Double Patterning (DP)
  - SMO and Contact Hole Imaging
  - EUV
- Alternative Lithography Manufacturing
  - Massively Parallel e-Beam
  - Nanoimprint
  - Through Silicon Vias (TSV)
- Moore’s Law & Lithography Manufacturing Roadmap

One Person's View – The coming of EUV maybe inevitable, the question is when …

- For foundries, the enabling of EUV lithography is entirely dependent on EUV mask infrastructure to become ready for volume manufacturing
  - At 2011/2012 – very unlikely to be ready for 22nm
  - At 2013/2014 – less uncertain for 15nm, still questionable (???)
  - At 2015/2016 – ArFi DP will completely run out of steam for 11nm
ArFi quadruple patterning (QP) is super expensive
- For foundries, EUV transition may happen at 2015/2016 pending on EUV mask infrastructure to become ready

Moore's Law will continue for the next 10 years…



It is not Moore's Law but the People who advance the technology.

Photo was taken with my iPhone at ITRI USA office in summer 2009.